High Speed Design of FPGA based Golay Encoder and Decoder

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ABSTRACT

In wireless communication systems the most important issue to be considered is the ability of the receiver to detect the errors and correct them from the received information, so as to provide correct information data to the processor. A number of different methods are available to implement the hardware and software with such preference. But, when the length of the communication link becomes very long, i.e., the distance between the wireless transmitter and receiver is very large, the effect of noise on the transmitted signal may cause a change in multiple bits of the transmitted information. This can cause drastic loss in many cases. In this brief a Field Programmable Gate Array (FPGA) based design and simulation of Golay Code (G23) and Extended Golay Code (G24) Encoding scheme are presented. This work is based on the optimization of the time delay of the operational circuit to encode a data packet using the Golay Encoder.

General Terms

Golay code, extended golay code, encoderAlgorithm, Decoder algorithm, Xilinx ISE

Keywords

Encoder, Decoder, FPGA, Operational Delay

1. INTRODUCTION

Communication is important in our daily life. We use phones, satellites, computers and other devices to send messages through a channel to a receiver. Regrettably, most types of communication are subject to noise, which may cause errors in the messages that are being sent. Especially when sending messages is a complicated or expensive task, for example in satellite communication, it is important to find ways to moderate the occurrence of errors as much as possible. This is the central idea in coding theory: what we have received and what message was being sent? To make this problem uncomplicated we use error-correcting codes. The foremost idea is to add redundancy to the messages which enables us to both recognize and correct the errors that may have occurred. This paper proposed a specific type of error-correcting codes, the extended Golay code G24.The information is transfer in three steps a source sends, a channel transmits, and a receiver receives. There is an option that at the time of transmission the information is altered to noise so to avoid this condition we use error correction codes. Fig. 1 show that a message is encoded into a codeword, it is sent to the receiver through a channel, in this channel the possibility exists that errors occur, and the receiver tries to obtain the original message by decoding the word.
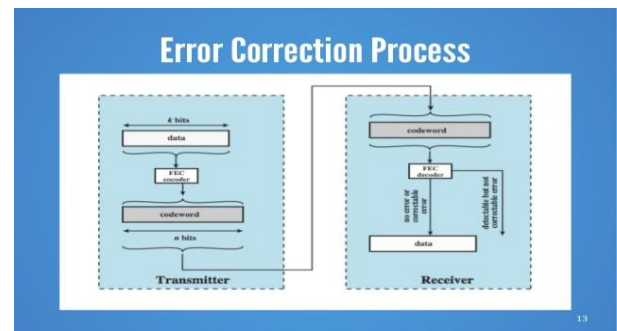

Fig 1:Process of Error Correction Code

Golay code is an error correcting code which is used to specifies that what we have received and what is send .some of the most important properties of such codes which allows us to give a detailed description of the extended Golay is :Firstly a message m of length k is a sequence of k symbols out of some finite field F, so m = (m1 : : :mk) belongs to F^k. Then an n-code C over a finite field F is a set of vectors in F^n, where n ≤ k. Since we will be commerce with a binary code only, we will assume codes are binary from now on. Second property says that the probability of error p is the probability that 1 is received when 0 was sent, or 0 is received when 1 was sent. Third property says that the hamming weight of a vector belongs to a function $F^n$is the number of its non zero elements. Fourth property says that the humming distance of two vectors belongs to a function $F^n$is the number of place where they differ. The idea is that an n-code C is a strict subset of F^nin which we want the Hamming distance between any two vectors to be as large as possible. Therefore, the min. Hamming distance is an important characteristic of the code. Fifth property says that the min. Hamming distance D of a code C is defined as D = min {dist (X, Y) I X, Y belongs to C} where C is the code. The description of work in this paper is as follows: Section-II gives an overview on the work performed by other scholars in Golay Code implementation and applications. Introduction on Golay code and its encoding algorithm is described in Section-III. Section-IV presents the simulation and synthesis results of the performed work. The conclusion based on the proposed work and the future work scope is presented in Section-V. In the last the references arementioned.

2. LITERATURE REVIEW

In reference [1] the proposed paper addresses error correcting phenomena using Golay code encoder. . A brief introduction and explanation of Golay coding scheme is presented in [3]. 4-bit Golay Encoder and Decoder design and implementation Based on FPGA is simulated in [4] using Xilinx ISE and Models in Tools. Reference [5] presents a soft algorithm based decoding orientation to hardware implementation of

(24, 12, 8) Golay code with implementation of the algorithm on FPGA. In [6] it is shown that the (24, 12, 8) Golay code is to be designed as a direct sum of two array codes that involve four component codes from which two are simple block codes Which are linear (repetition code and SPC code). Construction of Golay Code Complementary Sequences is presented in [7] for application of Golay Coding in the fields of physics, combinatory (orthogonal design and Hadmard matrices), surface acoustics and tele-communication. A better algorithm for decoding Golay Code is presented in [8] which uses one-to-one mapping between the syndrome "S1" and error patterns which can be corrected. In this proposed work the algorithm determines the error locations by using look-up tables without the multiplication operation over a finite field. This algorithm has been verified by the scholars on a C-language based software simulation platform. The work presented in [9] focuses on Golay code decoding using soft-in/soft-out and symbol by symbol APP (a posteriori probability) algorithm through co-set based technique. A study based on discussion on the error correction capability of MSK modulation with Golay code and BPSK modulation with Golay code is presented in [10], which concludes that Minimum Shift Keying Golay code is comparatively more robust. A technique based upon reversing the conventional scheme of Golay code (24, 12, 8) that maps 24-bit vectors into 12-bit message words is proposed in [11] to improve the search operation when multi-attribute objects are partially distorted. The work in [12] presents generation of Doppler Resilient waveforms using Golay Complementary sequence which have ideal ambiguity along the zero Doppler axis but are sensitive to non-zero Doppler shifts. The work in [13] showa Golay code transformation used for Ensemble Clustering that is usufull in application to Medical purposes. This method of cluster is unique to all other techniques because of its linear time complexity. Reference [14] presents an error correction Golay code for clustering large amount of data Streams with thw use of error correction Golay codes and this approach is used in the field where the requirement to accumulate multidimensional data. In Reference [15] the proposed methodology fulfill the requirement reducing the peak to average ratio (PTAR) with the help of special Fractional Fourier Transform (FRFT) followed to the low complicity Golay sequence coder in order to provide optimal de-correlation between signal and noise. To achieve the requirement of low complexity, low bit error rate and ratio of peak to average power. Reference [16] presents an Methedology for the implementation of Hardware of (24, 12, 8) Golay code in FPGA (Field programmable gate array) system. For removing the complexity of arithmetic operations this arises in the existing algorithm. The proposed algorithm chooses the absolute value rather than bit error probability to obtained better results as compared to the existing algorithms. Reference [17] proposes a new algorithm to fulfill the requirement of faster decoding for the Gosset Lattice, Golay code and Leech Lattice. The proposed design introduced two approaches to first when charge in of length n and taking soft decoding algorithm at an arbitrary point R^n in to the nearest code word and second a decoding algorithm for a lattice A in R^n changesan arbitral point of R^n into a closest lattice point.Reference [18]proposedan efficient soft-decision decoder of the (23, 12, 7) binary Golay code up to the four errors and almost all patterns of three errors and all fewer random error can be corrected with the help of proposed algorithm.

3. GENERATOR AND PARITY MATRIX OF(24,12) GOLAY CODE

A binary Golay code is represented by (23, 12, 7), In which the distance between two binary Golay codes is Represented by 7 and 12-bits is of massage bits and codeword is 23 bits long. It is necessary to construct binary codes in a Galois Field (GF). Binary field is denoted by GF(2), which supports different binary arithmetic operations.

The extended (24, 12) binary Golay code [1] which presents in this paper can correct three and less than three errors. With the help of the 11 x 11 Bc Matrix.. Because of Bc Which has the Property Of cyclic structure and also it is the component of both generator and the parity check matrices its procedure of decoding is very easy.

Genrator and Parity Matrix Of Golay Code

$$
Bc = \begin{pmatrix} b1 \\ b2 \\ b3 \\ b4 \\ b5 \\ b6 \\ b7 \\ b8 \\ b9 \\ b10 \\ b11 \end{pmatrix}
$$

Let Bc be 11*11 Matrix over Galois Fiels GF Where

$$b1 = 1,1,0,1,1,1,0,0,0,1,0$$

b2 is Obtained From b1 By Shifting Cyclically the Sequence b1 one Position to the Left, the Third row in Bc is Obtain in the same way,and so on.

$$
Bc = \begin{bmatrix}
1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\
1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\
0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 \\
1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \\
1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 \\
1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \\
0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \\
0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 \\
0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 \\
1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\
0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1
\end{bmatrix}
$$

The (24, 12) Golay code has the generator and parity check matrices as Follows.

$$G = \begin{bmatrix} B & I \end{bmatrix} \quad H = \begin{bmatrix} I & B \end{bmatrix}$$

,

where I - identity matrix 12 x 12,

$$B = \begin{bmatrix} Bc & j^T \\ j & 0 \end{bmatrix},$$

and

$$j = [1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1]$$

.

Therefore

$$B = \begin{bmatrix} 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 \end{bmatrix};$$

$$G = \begin{bmatrix} 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix},$$

$$H = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 0 \end{bmatrix},$$

It can be seen that ,,

$$B^T = B$$

$$B^2 = I.$$

$$B\,B^T = I$$

4. ENCODING AND DECODING OF (24,12) GOLAY CODE

Same in the case of any linear code, to generate a code vector it nessesary to multiply the vector i, which is having 12 information bits.

$$i = [i_1, i_2, i_3, i_4, i_5, i_6, i_7, i_8, i_9, i_{10}, i_{11}, i_{12}]$$

by the matrix: G

$$v = i\,G,$$

Wherefrom

$$v = [i_1 + i_2 + i_4 + i_5 + i_6 + i_{10} + i_{12}, i_1 + i_3 + i_4 + i_5 + i_9 + i_{11} + i_{12}, i_2 + i_3 + i_4 + i_8 + i_{10} + i_{11} + i_{12}, i_1 + i_2$$

$$+ i_3 + i_7 + i_9 + i_{10} + i_{12}, i_1 + i_2 + i_6 + i_8 + i_9 + i_{11} + i_{12}, i_1 + i_5 + i_7 + i_8 + i_{10} + i_{11} + i_{12}, i_4 + i_6 + i_7 + i_9$$

$$+ i_{10} + i_{11} + i_{12}, i_3 + i_5 + i_6 + i_8 + i_9 + i_{10} + i_{12}, i_2 + i_4 + i_5 + i_7 + i_8 + i_9 + i_{12}, i_1 + i_3 + i_4 + i_6 + i_7 + i_8$$

$+ i_{12}, i_2 + i_3 + i_5 + i_6 + i_7 + i_{11} + i_{12}, i_1 + i_2 + i_3 + i_4 + i_5 + i_6 + i_7 + i_8 + i_9 + i_{10} + i_{11}, i_1, i_2, i_3, i_4, i_5, i_6, i_7,$

$i_8, i_9, i_{10}, i_{11}, i_{12}].$

For decoding of the extended Golay code, shown below,need to determine the error pattern$u = v + w$,

where w is vector received and v the nearest w code vector. $wt(x)$ represents the weight of the vector x, (the number of "ones" presents in x),

bi- Is the i-th row of the matrix B,

ei- Is the word having length 12 and 1 in the i-th position and zero elsewhere. After calculating u Let we assume that the received vector which is corrected will be $v = w + u$.. the steps of the algorithm are as follows:

$$s = w\, H^T.$$

Step 1. Determine the syndrome(S)

Step 2. If $wt(s) \leq 3$ then

$U = [S, 000000000000].$

Step 3. If $wt(s + b_i) \leq 2$ for some b_i of B

then $U = $ S+bi ,ei

Step 4. Determine the second syndrome(SB)

Step 5. If $wt(sB) \leq 3$ the**n**

$U = [000000000000, SB].$

Step 6. If $wt(sB + b_i) \leq 2$ For some bi of B then $U = [$ ei,SB+bi $].$

Step 7. Retransmit the signal if U is not determine

5. SIMULATION AND SYNTHESIS RESULTS

The present work is simulated using Xilinx. The RTL Schematic diagrams of Encoder and Decoder designs are shown in Fig 2 and Fig 3 respectively.

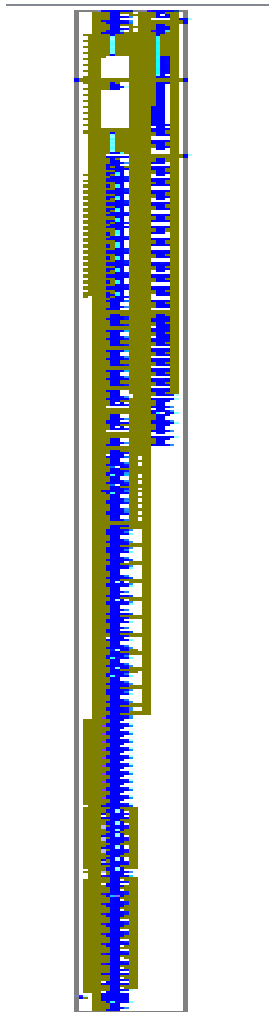**Fig:2 RTL Schematic Diagram of Proposed Golay Code (24, 12, 8) Encoder**

Fig :3 RTL Schematic of Proposed Golay Code (24, 12, 8) Decoder

The Encoder and Decoder simulation waveforms are shown in Fig4 and Fig 5 respectively. A 12-bit data is used to encode using the proposed encoder.. The FPGA based hardware

utilization summary of the proposed Encoder and Decoder designs is presented in Table-I and Table-II respectively.

Table 1.Hardware Utilization Summary of Encoder

Vertex-IV XC4VLX160 -12FF1148	Total	12-bit Golay Encoder	
		Used	%
Slices	67584	40	0
Flipflops	135168	53	0
LUTs 4-Inputs	135168	72	0
Bonded IOBs	768	39	5

Table 2.Hardware Utilization Summary of Decoder

Vertex-IV XC4VLX160 -12FF1148	Total	12-bit Golay Decoder	
		Used	%
Slices	67584	196	0
Flipflops	135168	151	0
LUTs 4-Inputs	135168	367	0
Bonded IOBs	768	87	11

Table-III represents a comparative analysis of the delay based results of the proposed work with some existing works.

Table 3.Comparison of Dynamic Power Consumption of Proposed Design

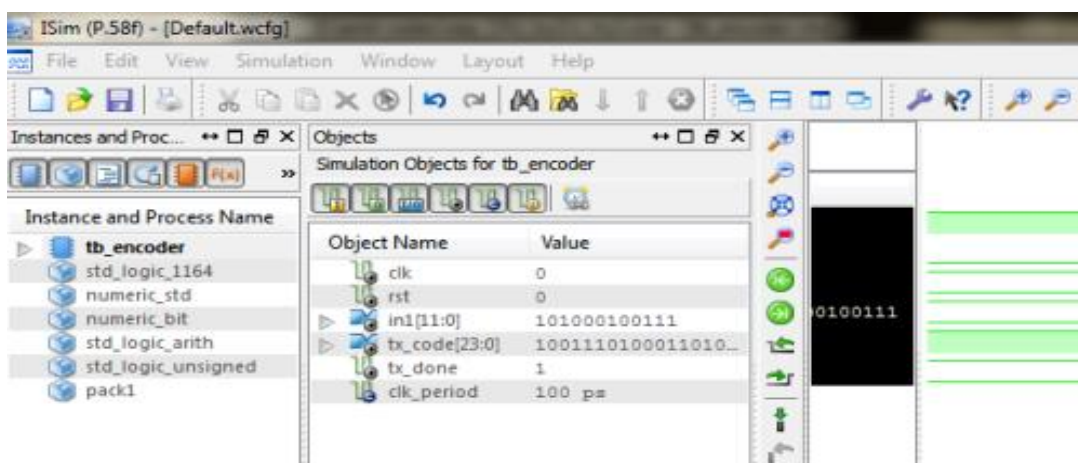| Work	Operational Frequency (MHz)	
	Encoder	Decoder
Proposed	333.206	89.123
[1]	238.575	80
	-	

Fig 4 Encoder Simulation Waveform for Proposed Golay Code (24, 12, 8)
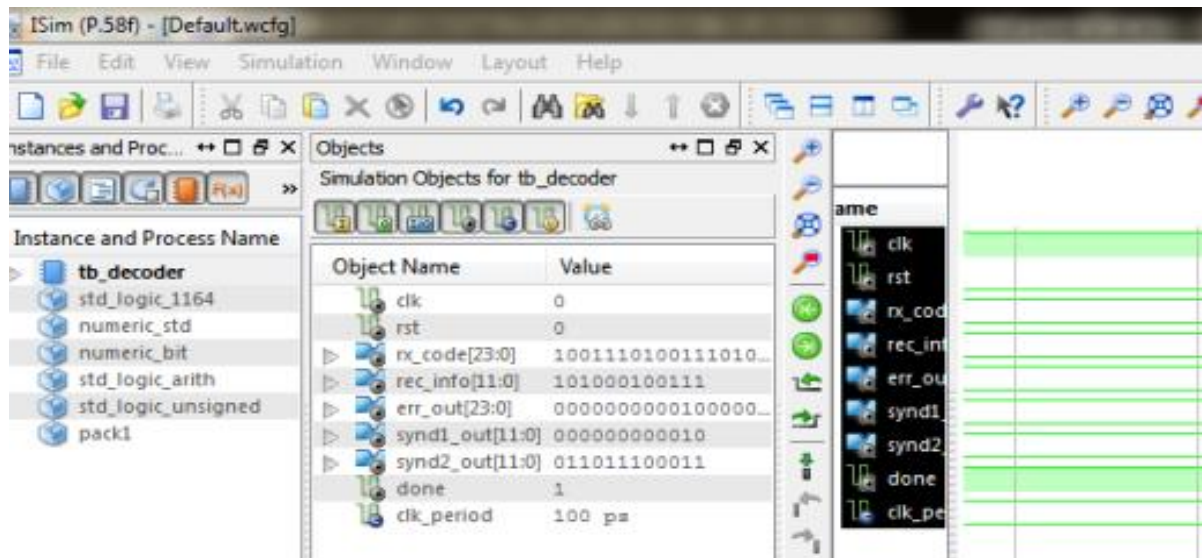
Fig5: : Decoder Simulation Waveform for Proposed Golay Code (24, 12, 8)

6. CONCLUSION

Hardware architecture for extended binary Golay encoder and decoder for High speed Implementation are designed and simulated in the proposed work. The results obtained from the design synthesis for encoder and decoder supersedes the reference schemes in term of the operational frequency. This makes the proposed design a good option to be used in the high speed application based configurable circuits. In future there is a great scope to further optimize the performance of the proposed algorithm. In future the scholars may undertake the challenge to reduce the ratio of overhead bits versus data bits in the encoded codeword. Or the researchers might increase the length of the data word that can be encoded using the same algorithm with the same or better error detection and correction ability.

7. ACKNOWLEDGMENTS

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