Abstract

With the continuously growing quest for miniaturization of circuit technology, one of the prime focuses of the research has shifted in the direction of ultra low power circuit designs. As the size of chips is shrinking and the density is increasing simultaneously, losses are increasing mostly in the form of power dissipation. Based on various parameters of performance evaluation in a VLSI circuit and the continuously growing quest for highly efficient and ultra shrunk devices, has compelled the researchers and designers to come up with improved designs which are highly efficient and feasible. In this Paper we have calculate leakage power at different input vector combination with different technology to identify the effect of channel length reduction in CMOS technology. All simulation is performed over on Conventional NAND gate with variation of transistor by using Berkley Predictive Technology Mode at 65nm technology by using HSPICE simulator and analyse in terms Power consumption, delay and PDP with supply voltage of 1V at 100MHz frequency.

References
Calculation of Leakage Current in CMOS Circuit Design in DSM Technology


Index Terms

Computer Science               Circuits and Systems

Keywords

Low Power, Variation in NAND Gate, CMOS, GIDL, PDP.