Abstract

This paper presents low-power characteristics of adiabatic complementary pass-transistor logic (ACPL) using four-phase AC power supply. Adiabatic CPL circuits consist of pure NMOS transistors, use CPL blocks for evaluation and bootstrapped NMOS switches to eliminate non-adiabatic loss of output loads. In this paper, combinational circuit (4-bit ripple carry adder) and sequential circuit (4-bit binary counter) is realized with adiabatic CPL. These combinational and sequential circuits have been simulated in CADENCE design tool at 90nm technology and simulation results shows that the adiabatic CPL 4-bit ripple carry adder achieve power savings of 80% with PAL-2N logic and adiabatic CPL 4-bit binary counter achieve power savings of 52% with CMOS logic for clock frequencies from 50 to 300 MHz.

References


**Index Terms**

Computer Science  
Power Systems

**Keywords**

Adiabatic CPL; Combinational circuits; Sequential circuit; Low-power; VLSI