Abstract

Now a day's low power SRAMs have become a critical component of many VLSI chips. This has especially true for microprocessors, where the demanding on chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processors and the main memory. Simultaneously, power dissipation has been becoming an important factor to recognise due to the increased integration and operating speeds, as well as due to the explosive growth of battery operated applications. In this paper we have compared 4T, 6T, 7T, 8T and 9T SRAM cell at 65nm and 45nm technology by using HSPICE simulator and analyse in terms Power consumption, delay and PDP with supply voltage of 1V at 100MHz frequency.

References


Index Terms

Computer Science

Circuits and Systems
A Comparison of n-T SRAM Cell in Nanometre Regime

Keywords

SRAM, SNM, Power consumption, PDP.