Abstract

Multipliers being the key components of various applications and the throughput of applications depends on Arithmetic and logic units (ALU), Digital signal processing blocks and Multiplier and accumulate units. Vedic Multiplier has become highly popular as a faster method for computation and analysis. So that the latency of conventional multiplier can be reduced. Here the vedic mathematic Sutra- ‘Urdhva Tiryagbhyam’ and Nikhilum are used for efficient multiplication. The main parameters for improvement are speed, delay, hardware complexity. From this review, the conclusion regarding how well a challenge has been solved, and recognize prospective research areas that require auxiliary effort.

References

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2. Shishir Kumar Das1 and Ankit Kumar Singh2 “Design and Implementation of Low Power Multiplier Using Vedic Multiplication Technique”


Index Terms

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