International Journal of Computer Applications (0975 - 8887)
Volume 155 - No.8, December 2016

Design and Implementation of High Speed Multiplier based on Vedic Mathematics: A Review

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ABSTRACT

Multipliers being the key components of various applications and the throughput of applications depends on Arithmetic and logic units(ALU), Digital signal processing blocks and Multiplier and accumulate units. Vedic Multiplier has become highly popular as a faster method for computation and analysis.So that the latency of conventional multiplier can be reduced. Here the vedic mathematic Sutra- 'Urdhva Tiryagbhyam' and Nikhilum are used for efficient multiplication. The main parameters for improvement are speed, delay, hardware complexity. From this review, the conclusion regarding how well a challenge has been solved, and recognize prospective research areas that require auxiliary effort.

Keywords

Vedic multiplier, Nikhilum, Urdhva Tiryakbhyam

1. INTRODUCTION

Multiplier is an essential functional block of a microprocessor because multiplication is needed to be performed repeatedly in almost all scientific calculations. The fast and low power multipliers are required in small size wireless sensor networks and many other DSP (Digital Signal Processing) applications. They are also used in many algorithms such as FFT(Fast Fourier transform), DFT(Discrete Fourier Transform) . There are two basic multiplication methods namely Booth multiplication algorithm and Array multiplication algorithm used for the design of multipliers. The schemes for efficient addition of partial products are Wallace tree ; Dadda tree . The speed of multiplication (as well as power dissipation) is dominantly controlled by the propagation delay of the full / half adders used for the addition of partial products.Multipliers have large area, long latency and consume considerable power. Vedic multiplier architecture achieves high speed, low area and less power consumption. The implementation of multiplier using vedic mathematics is carried out. As the existing methods have their own limitations there are different approaches which use Vedic mathematics . Vedic mathematics is an ancient and long back introduced method of mathematics which is really a good method to overcome various complex mathematical calculations by executing simpler steps. It was discovered again by an talented mathematician- Sri Bharati Krishna Teerthaji Maharaja (1884-1960) who divided the Vedic mathematics into sixteen easy sutras, that are:

Ekadhikina Purvena	By one more than the previous one Nikhilam
Navatashcaramam Dashatah	All from 9 and the last from 10
Urdhva-Tiryagbyham	Vertically and crosswise
Paraavartya Yojayet hline Shunyam Saamyasamuccaye	Transpose and adjust When the sum is the same that sum is zero.
(Anurupye) Shunyamanyat	If one is in ratio, the other is zero
Sankalana-vyavakalanabhyam	By addition and by subtraction
Puranapuranabyham	By the completion or non-completion
Chalana-Kalanabyham	Differences and Similarities
Yaavadunam	Whatever the extent of its deficiency
Vyashtisamanstih	Part and Whole
Shesanyankena Charamena	The remainders by the last digit
Sopaantyadvayamantyam	The ultimate and twice the penultimate
Ekanyunena Purvena	By one less than the previous one
Gunitasamuchyah	The POS is equal to SOP
Gunakasamuchyah	The factors of the sum is equal to the sum of the factors

2. LITERATURE SURVEY

In may 2016 Rakesh M *et al.* proposed an efficient 64 bit multiplication is implemented making use of VEDIC multiplier to extend the ease of computation as compared with conventional method. Here they designed the architecture of Vedic multiplier with less number of gates and high speed specification. The 32 bit multiplicand and multiplier divided into MSB and LSB bits each of length 16 bit and this is implemented in given 16X16 block multiplier. Xilinx Synthesis 16.1 tool is used for synthesis purpose. The four 32 bit Vedic multipliers and two modified carry save adder are required to realize 64 bit multiplier. The proposed architecture is very fast and accurate[1].

In april 2016 K.N.Vijeyakumar *et al.* worked to develop and design high speed along with area efficient Arithmatic unit suitable for high performance speed. This provides the suitability for the proposed AU to gain high speed portable VLSI implementation. Note that the structuring of our proposed AU with equal logic depth maintains parallelism and uniform delay across all the outputs. In addition the design of the blocks and multiplexers are such that the design can be reconfigured for higher bitwidths of input operand with ease.[2]

In april 2016 Shraddha Wanjari *et al.* worked on designing and implementation of adder using DKG gate reversible logic.There is no power dissipation if a circuit contains only reversible gates. The register designed in the accumulator is used to add the multiplied numbers. MAC unit is formed by the multiplier, adder , accumulator.To obtain the final multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensity the action of the MAC Unit. The suggested MAC is compared with the conventional MAC and the results are analyzed. The results obtained using there design had better performance when compared to the pervious MAC designs [3].

In april 2016 Shiksha Pandey *et al.* presented the design and implementation of high speed 16x16 bit Vedic multiplier architecture which is some what different from the Conventional method of multiplication like addition and shifting. The implementation and simulation of Verilog HDL code for Urdhva tiryakbhyam Sutra for 16x16 bits multiplication and carry select adder is carried on XilinxISE9.2i. There is reduction in area in FPGA and also improve the performance in terms of speed. It will be verified by comparing it will hardwired unsigned multiplier.[4]

In February 2016, Arunkumar P. Chavan *et al.*,has worked on two multiplier using kogge stone adder and ripple carry adder respectively. The modelling used for multiplier was verilog HDL and synthesized Using Cadence Digital Complier (DC) . Here 45nm technology was used . The synthesized netlists were loaded into Cadence SOC Encounter to carry out RTL to GDSII code. Processing time was decreased therefore the advantage of high speed was acquired.[5]

In february 2016 Pankaj Prajapati *et al.*, Used nikhilam sutra and barrel shifter for implementation of multiplier. The offered multiplier has fast response, least area and cosumed power. The barrel shifter reduced the delay when compared to conventional multipliers. The designe is being developed on Xilinx 14.1i updated version. Xilinx 9.2i has features like low memory requirement, fast debugging, and low cost. The design provides 27% low memory. ISE 14.1i software features gives sudden advancements in place and route and clock algorithm providing up to a 15% performance advantage.[6]

In january 2016 Suryasnata Tripathy has carried out work on low power multiplier using vedic mathematics. using Cadence EDA tool designs were realized in 45 nm CMOS Process technology . In this design the multiplier block consists of chain of AND gates for partial product terms generation and adder is used for adding them.Due to long addder tree structures,latency is increased in conventional multiplier so speed is limited.The design offers low power multiplier architectural design based on Vedic mathematics for computing high speed and area is reduced.The adder chains used in the multiplier units comprise of 14T full adders and 9T half adders designed for low power and high speed calculations. This topologies results in reduction of area requirement. As the critical path contains few number of transistors, the total delay is minimized.In this proposed design new topologies for 4bit and 8 bit architectures are designed based on UT sutra of Vedic mathematics. [7]

In 2015 Bhavesh Sharma *et al.* designed and modified architecture to ensure better aspect of area, power , power delay product and power density . Although with a slight increase in delay we achieve a low power and area architecture. This is a known composition between power and speed or delay which states that as the speed increases delay decreases. In the modified architecture the power delay product is reduced by 14.91% and the power density is reduced by 18.21%.The increase in delay is 15%.This architecture uses 9.5% less area compared to previous one. There is reduction in power consumption of 26%. [8]

In may 2015 Pranita Soni1implemented the 16 bit ?Vedic Urdhva Tiryagbhyam? Multiplier and Booth Multiplier. In Xilinx software these algorithms are syntesized and executed in VHDL language by using model sim. FPGA development board from Spartan 3 family is used for hardware implementation of these algorithms. As partial product and their sum calculated simultaneously the vedic multiplier is independent of clock frequency. Thus it doesn?t require high clock frequencies for multiplication and due to this less switching takes place, providing less switching delay and power minimization and thus results in an efficient processor in delay and power. The programming is divided into 4 parts. For developing the multiplier of 16X16 bit, they first develop the multiplier of 2X2, 4X4 and 8X8.[9]

In march 2015 Amit Bakshi *et al.* designed four multipliers that are array multiplier , booth multiplier , radix4 vedic multiplier , wallance tree multiplier. If the requirement of the application is of an efficient multiplier then booth multiplier (radix 4) may be used, and if the requirement is for low power then vedic multiplier is to be used . The vedic multiplier has a better power delay product and power density compared to booth multiplier [10].

In june 2014 Mrs.Toni J.Billore *et al.* used a 8-bit Vedic multiplier utilizing quick viper improved as a part of terms of proliferation postponement when contrasted and ordinary multiplier. The implementation of code done on Altera Cyclone FPGA device. The delay of 6.781ns is achieved in design using barrel shifter block in base selection module and multiplier of architecture used. 8-bit barrel shifter used, requires one and only clock cycle for ”n” number of movements. The configuration of 8 bit Vedic multiplier utilizing barrel shifter is executed and confirmed utilizing FPGA and ISE Simulator. The center utilized here was actualized on Altera Cyclone II 2C20 FPGA gadget programming.Around 75% of delay reduction can be observed from the proposed design with respect to array multiplier, whereas the conventional Vedic multiplier contributes to 43% of reduction in delay with respect to array multiplier.[11]

In september 2013 C.Sheshavali *et al.* , implemented a multiplier on a Cyclone III FPGA. The proposed multiplier is 1.5 times faster than the other multipliers for 16x16 and consumption of 76% area for 8x8 multiplier and for 16x16 multiplier only 42% area. Here all the partial products are generated in parallel. So the speed of the multiplier is higher compared to array multiplier. the proposed multiplier is best suited for the applications where the less area requires and speed is major considerations. This is achieved due

to the feature of multiplier that will consume only fewer logic elements for its implementation.[12]

In march 2013 Pavan Kumar U.C. *et al.*, described and implemented 8-bit Vedic multiplier enhancing in terms of propagation delay while compared with array multiplier, Braun multiplier, modified booth multiplier and Wallace tree multiplier. They utiliized 8-bit barrel shifter. FPGA and ISE Simulator is used for design implementation and verification. Xilinx Spartan-6 family xc6s1x75T-3-fgg676 FPGA was used for code impiementation. The design could achieve propagation delay of 6.781ns.[13]

In march 2012 G.Ganesh Kumar *et al.* had proved the coherency of Vedic sutra-Urdhva Triyagbhyam for multiplication that state the difference in the conventional method of multiplication. At a same time it also generates the intermediate products and unwanted multiplication steps are eliminated with zeros and also using Karatsuba algorithm, scaled higher bit levels with the compatibility to different data types. Urdhva tiryakbhyam is most wated Sutra (Technique) for to get higher efficiency, providing least delay for multiplication. Further, the Verilog HDL coding for 32x32 bits multiplication using Urdhva tiryakbhyam Sutra and their FPGA implementation is done using Xilinx Synthesis Tool on Spartan 3E kit and output has been displayed on LCD of Spartan 3E kit. The computational time required for calculating the product of 32x32 bits is 31.526 ns. The proposed multiplications were implemented using two different coding techniques viz., conventional shift & add and Vedic technique for 4, 8, 16, and 32 bit multipliers. It is observed that there is effective increase in speed of the Vedic architecture. [14]

Aniruddha Kanhe *et al.* ,The proposed Vedic Multiplier's implementation was done using VHDL and the ModelSim and ISE simulation software is used for functional verification of each block. The basic blocks used to build are two input AND gate and one Adder, the structural modeling style is used for implementingVedic Multiplier. VHDL code is used for multipier's implementation.The idea of BIST(Built in self test) is to design a circuit that can verify itself and found whether it is ?good? or ?bad?.The mechanism to determine the output responses of the circuit under test (CUT) additional circuitry is required whose functionality must be capable of generating test patterns correspond to that of a defect free circuit . Delay for proposed multiplier is 6.801 ns and power dissipation is 31mw.[15]

S. S. Kerur *et al.* proposed multiplier in which, Coding technique used is VHDL and Xilinx ISE series is for synthesis purpose. It has increased performance in the DSP system was carried out using ModelSim ISE 6.0 and the functional verification through simulation of the VHDL code. The multiplier is specially designed for speed and area using Xilinx, device family Spartan3, package pq208, and speed grade -4. the delay for 8-bit vedic multiplier is 24.16ns and for 16-bit vedic multiplier is 36.563 ns. This vedic multiplier designed to get area or space efficiency .Here 86.71% lesser time slices are required and also around 88% lesser four input LUT are used for Vedic multiplier . The utilization of bonded IOBs is 64.48%. From the report, it can decide that by reducing gate delay by factor 24% 8 bit Vedic multiplier has advantage of higher speed as compared to array multiplier and near about 18.2% compared to booth multiplier. Similarly, by reducing gate delay by factor of 39.9% 16 bit Vedic multiplier has advantage higher speed as compared to array multiplier and around 48.36% compared to booth multiplier.[16]

In MAY 2016- Rakesh M *et al.*, proposed an efficient VEDIC multiplier for to do 64 bit multiplication for simplification of operation comparing with the existing algorithms. Designed the Architecture of Vedic multiplier with minimum no. of gates and high speed characteristics. Xilinx XST is used to Synthesis the Implemented multiplier.This paper presents the advanced way of implementing high speed multiplier using Urdhva Tiryagbhyam sutra and CSA (Carry Save Addition) technique. A modified multiplier for 32 bit is designed. The 64 bit multiplier is implemented using four 32 bit Vedic multipliers and two modified CSA(carry save adder). Vedic mathematics deals with techniques of arithmetic reminiscent of normal maths.[17]

In 2016-G.Challa Ram *et al.* ,Proposed multiplier Using XILINX software 12.2 a Verilog HDL code for vedic multiplier is simulated and synthesized on Spartan 3E kit. And the designed array multiplier was compared with the earlier proposed multiplier in terms of delay, memory and power consumption. Afterwards the 8x8 Vedic multiplier is used as basic building block for implementing of 16x16 multiplier. To reduce the overall and power consumption and requirement of gates compared to normal Vedic multiplier BEC(Binary to Excess Convertor) is used.Here Verilog HDL code for 16x16 bit Vedic multiplier is implemented on FPGA device xc3s500-5fg320 of Spartan 3E family. Result shows that for 8bit, memory utilized for Vedic multiplier using BEC is 138728KB, which is less as compared to Vedic multiplier that required 198568KB. Similarly for 16bit, memory utilized for Vedic multiplier using BEC is 139624KB, is less while comparing it whith normal Vedic multiplier that requirs memory of 208268KB.[18]

In 2016-R. Anitha1 *et al.*, focused on achieving higher speed and low power in implementation of Linear convolution algorithm using Vedic Sutras. The Verilog is used to implement the multiplier , using Cadence simulation is done with the help of Xilinx , and RTLcompiler isused for doing synthesis. Operations on complex numbers as well as for convolution this multiplier is used . The proposed design is limited to 8 Bit inputs only. The technology used for synthesis is 45 nm. The proposed design uses the Vedic algorithms to gain higher speed. The design requires 52% lesser area as compared to the conventional methods and it requires 71.234% lesser power . [19]

Himanshu Thapliyal *et al.* worked on basis of ancient Indian Mathematics,based on that square architecture for multiplier was proposed for low power and high speed applications. It generates all partial products and their sums in only one step. Synopys FPGA Express is used to synthezise the code using: Xilinx, Family: Spartan Svq300, Speed Grade: -6. This paper refers to improvement in power and speed over multiplication and square algorithm implemented in coprocessors in the field of math coprocessors in computers.Here as 8*8 to 16*16 bits increases so time delay is reduced. For the Xilinx, Vedic multiplier for 16x16 bit number the gate delay is 46 ns, 91ns for array multiplier and 225 ns for Booth multiplier in spartan family. And the numbers of HMAP & FMAP are 527 for array multiplier, 621 for Vedic multiplier and 1300 for Booth multiplier. For Spartan family Vedic square for 4 x 4 bit number the gate delay is 11 ns and the gate delay in Vedic as well as array Multiplier are 27ns and 23 ns respectively. The area of Vedic square are 11 and for Vedic and array they are 33 and 26 respectively.[20]

InApril 2016 -Aunnaty Puri1 *et al.*, presents the modified architecture of the Urdhava Tiryakbhyam hardware in order to reduce area and delay to improve overall performance by using modified Wallace tree addition. Due to reduction of the Wallace Tree the proposed work shows improvements in terms of on chip silicon area and speed efficiency as the amount of half adders and full adders used are less . The code for 16 bit Floating Point Unit using VHDL and Synthesized on Xilinx ISE version 14.5i simulation tool and target tool is Virtex -4 FPGA.[21]

In June 2012-Aniruddha Kanhe1 *et al.*, presents the basic design and implementation of the Vedic Multiplier using Urdhva tiryakbhyam and Nikhilam sutras.The basic building blocks of this multiplier are two input AND gate and Adder, for the implementation of Vedic Multiplier the structural modeling style is used.The performance of proposed multiplier is compared on the basis of area,power and speed.These multipliers are implemented using VHDL and the multipliers are synthesized using Xilinx ISE tool and Spartan 2E FPGA is used.[22]

In MAY 2016-Kaustubh Manikrao Gaikwad *et al.*, had deal with design and implementation of efficient high speed 16x16 multiplier using Vedic operators and used various algorithms like array & booth. On the basis of speed, area and power - multipliers were compared. The selected Device is 3s100evq100-5 and number of time Slices are 14 out of 960 1%. Number of 4 i/p LUTs are 25 out of 1920 1% and number of bonded IOBs are 16 out of 66 24%. Atmost the combinational path delay is 11.847ns.Here Total memory used is 150260 kilobytes. [23]

In 2011-S. S. Kerur *et al.*, had attempt to advances the design space for implementation of Vedic multiplier using VHDL efficiently. 86.71% lesser slices and also 88% lesser four input look-up (LUT)are used for Vedic multiplier. The utilization of bonded IOBs is 64.48%. Reduced gate delay by 24% as compared to array multiplier 8 bit Vedic multiplier gains higher speed and 18.2% compared to booth multiplier . Also, 16 bit Vedic multiplier gains higher speed by reducing gate delay by factor of 39.9% compared to array multiplier and around 48.36% compared to booth multiplier. [24]

In MAY 2016-Nitesh Kumar Sharma1 *et al.* ,designed multiplier on Xilinx-14.1 and simulated on Modalsim. Application analysis was done on Matlab for Sable Edge Detection application. Image quality analysis was done by PSNR, SSIM. Here hardware analysis is done on Vertex 6 FPA uses 45nm based technology. Approximately 20-30% reduction in logic block, delay, & frequency is achieved.The key contribution of this work is to develop a SPAA aware error tolerant Multiplier Unit. The proposed Multiplier unit was designed so that less area and power as well as high speed can acquire.[25]

Table 1. Comparison of Delay reported by Previous Approaches

	8*8 bit	**16*16 bit**
Array multiplier	32.01 ns	60.928 ns
Booth multiplier	29.549 ns	70.809 ns
Vedic multiplier [5] (BEC)	23.18 ns	38.87 ns
Vedic multiplier [7] (VHDL)	27 ns	46 ns
Vedic multiplier [11]	24.16 ns	36.563 ns
Vedic multiplier [25] (Barrel shifter)	6.781 ns	
Vedic multiplier [12] (Divide and conquer approach)	9.998 ns	

3. CONCLUSION

The purpose of this survey is to study existing methods used for multiplication using vedic maths techniques to gain better performance in terms of high speed, low power consumption and small area, also to identify the outcomes and shortcomings of the earlier work. It has been observed that in recent years many researchers have use Urdhva Tiryagbhyam sutra for the multiplication purpose. This survey identifies challenges that have not yet been resolved. In turn, this will help researchers in this area focus their research effort on those issues identified as bottlenecks and to eventually develop better multiplication techniques.
Multiplier requires in the different applications can be implemented using vedic mathematics.
Power, Speed and area are the three main impelling parameters which decides the system performance. Various techniques such GDI can be used to gain less power, reduce transistor count which will improve the performance.

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