20 Tap Reconfigurable IIR Filter using Fully Parallel MAC Algorithm

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ABSTRACT
The paper introduces designing of MAC 20 tap IIR filter based on Field Programmable Gate Array (FPGA).The implementation is based on Multiply Add and Accumulate algorithm (MAC) unit which plays important role in many of the DSP aplications.MAC unit is used for best performance digital signal processing system. The designed filter has been synthesized on Digital Signal Processor (DSP) slice based FPGA to perform multiplier function of MAC unit. The proposed filter is implemented on two FPGA devices Xilinx's Spartan-3E, xc3s500e-4fg320 and Vertex 2P, xc2vp30-5ff896 and compared on the basis of Direct-form I IIR and Direct–Form II IIR structure for hardware resource utilization as well as speed. The hardware result shows that the proposed low pass butterworth filter designed on spartan3E with Direct I Form 19.03% faster than that designed on vertex2p with Direct form II structure.

General Terms
VHDL, MAC, ISE

Keywords
IIR low pass Butterworth filter, Matlab, Xilinx, FPGA, Spatan3E, Virtex2P

1. INTRODUCTION
For computing DSP, especially the multiply accumulate operation is a common step that calculates the product of two numbers and adds the same product to the accumulator. In digital signal processing convolution, correlation and transformation are the three fundamental operations. In convolution multiply-accumulate operations are widely used. The MAC unit is independent of the CPU operation, it decreases CPU load and processes the data separately. In digital signal processing, digital filters are used widely. Digital filter is dominant tool of DSP [2].

In this paper IIR Butterworth filter is designed. Filters are used to eliminate unwanted signals and gives us the desired output signals. There are two types of filters: analog and digital. In order to design digital IIR filter, firstly analog Filter is designed and then by using these analog filters, Digital filters is realized. The implementation becomes quite easier when digital filters redesigned using analog filters. Digital filters are insensitive to high linearity and noise high Accuracy. Analog filters are designed using analog components like resistor (R), capacitor(C), inductor (L).There are two types of digital filters: FIR(Finite impulse response filters), IIR(Infinite impulse response Filters.) It is observed that if there is need for the linear phase characteristics within the pass band of the filter, FIR filters are used in that cases. However if there is no requirement for the linear phase characteristics, then any of the IIR or FIR filter can be employed. An IIR filter has lower side lobes in the stop band than an FIR filter having the same number of parameters. If some of the phase distortion is not tolerable, then an IIR filter is more preferred than FIR filters. Also its implementation involves fewer parameters, requires less memory and has lower computational complexity.

The important advantage of IIR filter on FIR filter is its implementation efficiency. IIR filters require less orders as comparison to meet same specification. A great part of digital technology deals with digital signal processing. This aspect in engineering has gained increasing interest, especially with much of the world now turning to wireless technology. FPGAs are essentially arrays of uncommitted logic and signal processing resources [2]. FPGA provides more logic flexibility and the power consumption is low. Programmable logic components and programmable interconnects are present in semiconductor FPGA.

2. IIR FILTERS
IIR stands for Infinite Impulse Response. Digital IIR Filters are used in many application such as high speed and low Power communication transceivers. [5] IIR Filters are infinite response filter, they have impulse response of infinite duration. Methods used to design analog IIR filter - Butterworth filter approximation, Cheyshev filter, Elliptic filter [3].Method used to design digital IIR Filter are Bilinear transformation, impulse invariance method, Matched Z transformation [3]. The bilinear transformation method is used to design the IIR filter. Firstly, analog IIR filter is designed using Butterworth filter approximation, cheyshev filter approximation, and elliptic filter approximation and then the analog IIR filter is converted into digital IIR filter using bilinear transformation approximation [6]. IIR filter design types - Low pass (LP), High pass (HP), Band pass (BP), Band stop (BS) filter with different settings in order, pass band frequency and stop band frequency, stop band attenuation while pass band ripple kept fixed [5, 6].

Generally IIR systems are recursive type. A recursive system means feedback connection is present from the output side to the input side. That means output signal is fed back to the input signal. This feedback connection is required to generate infinitely long impulse response. For the realization of IIR system present, past, future samples of input and past value of outputs are required. Matlab gives the opportunity to standardize and convert our coefficients in fixed point and also to test the effect optimization of IIR filter through the different settings available in matlab and reduce the errors caused by quantization of IIR filters and it also increase the performance of IIR filter. [6] IIR filter requires lesser no of arithmetic operation and these have lower computational complexity and smaller memory requirement.

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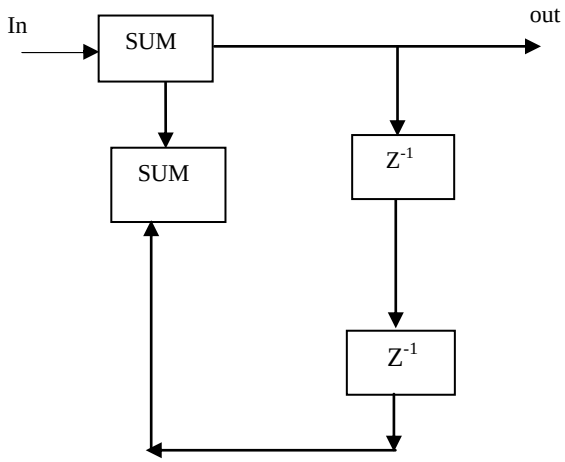

Fig 1. Block diagram of IIR filter

Transfer function of IIR filter is written as

$$H(z) = \frac{\sum_{k=0}^{N} b^k z^{-k}}{1+\sum_{k=1}^{M}(a_k+z^{-k})}$$

For the designing of IIR filter, it is necessary to find suitable value for the coefficients a_k and b_k to obtain the desired frequency response and magnitude response [5].

3. MATLAB FILTER DESIGN

Magnitude response, phase response, impulse response and step response of Butterworth low pass IIR filter obtained in Mat lab. This section has been designed and simulated using mat lab. Low pass Butterworth IIR filter is being designed using mat lab [8].

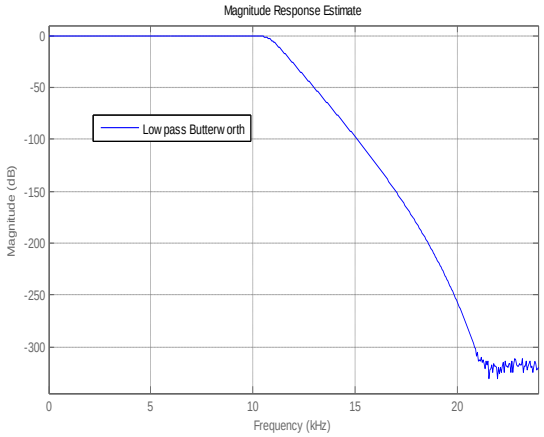

Fig 2. Magnitude Response of IIR

Magnitude response is graph between magnitude of transfer function with respect to frequency and magnitude plot represent magnitude of low pass butterworth quantized because all coefficients are quantized to fixed point by MATLAB.

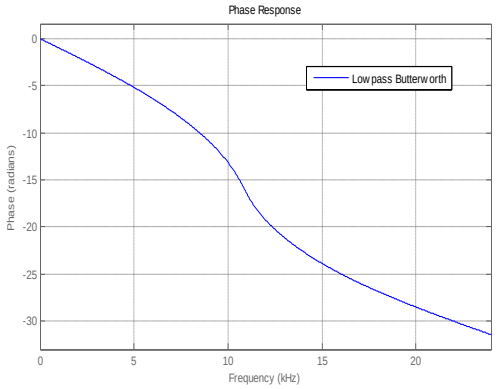

Fig 3. Phase Response of IIR

Phase plot of filter is approximate linear it represent that there is no phase distortion and time delay

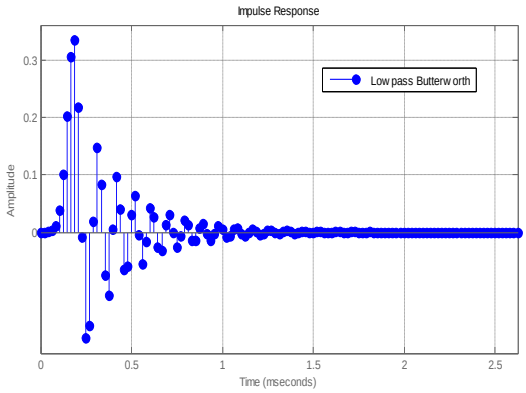

Fig 4. Impulse Response of IIR

Impulse response represent transfer function of system and if transfer function of filter is absolutely summable because it decrease as we move away from zero so it is stable digital filter.

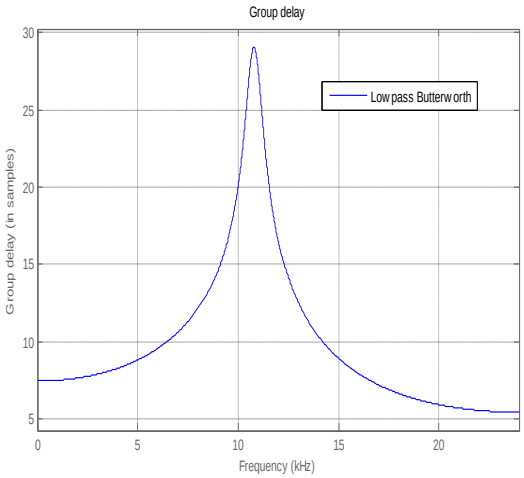

Fig 5. Group Delay of IIR

Group delay is the time delay of the amplitude envelopes of the various sinusoidal components of a signal through a device under test, and is a function of frequency for each component

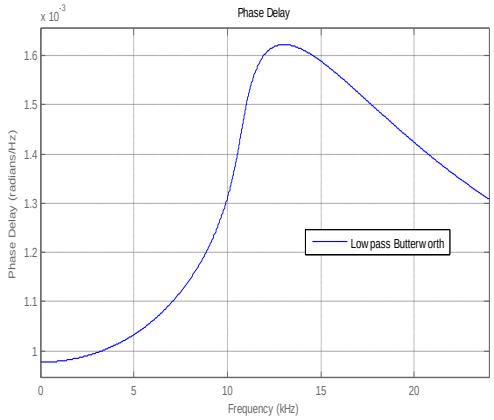

Fig 6. Phase Delay of IIR

Phase delay, in contrast, is the time delay of the amplitude envelope.

4. SYNTHESIS ON HARDWARE

The proposed low pass filter design synthesize with Xilinx 10.1 targeting a FPGA device Spartan 3E and Virtex-2P and device utilization summary and speed is compared. This section includes, VHDL code for designing of IIR filter and its implementation using MAC algorithm. Structure of proposed MAC based IIR filter is shown in Fig. 7.

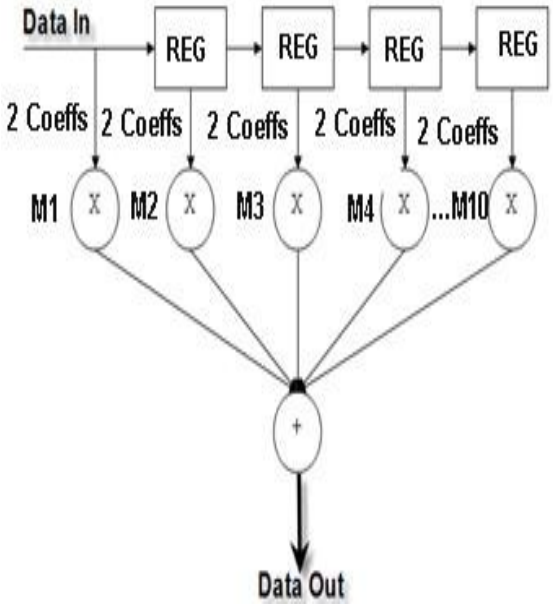

Fig. 7 MAC based IIR Filter

For observing the speed and resource utilization of designed IIR filter, the IIR filter has been synthesized on Virtex 2p based XC2VP30-5 FPGA device and Spartan 3E based xc3s500E-4 FPGA device.

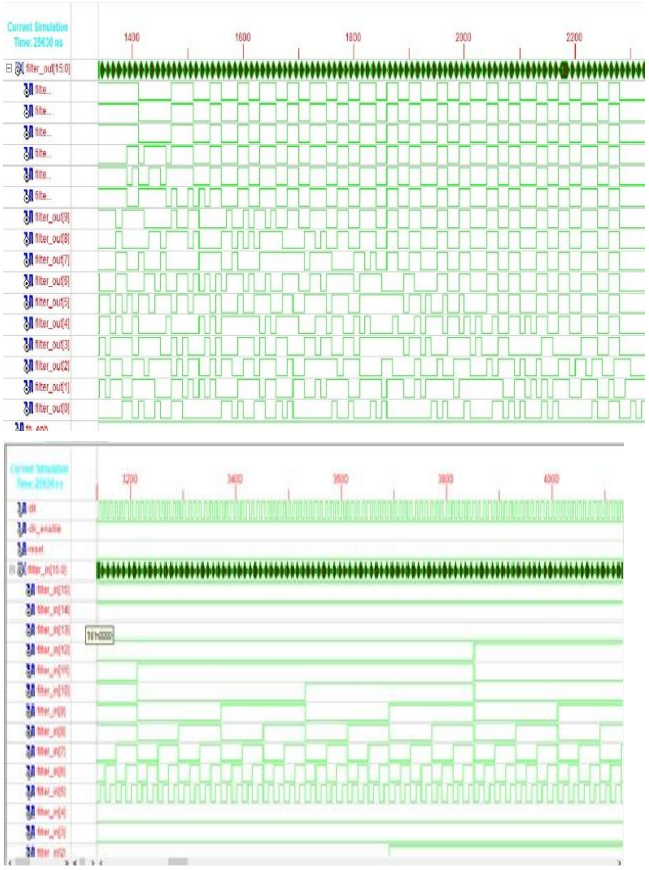

Fig 8. Test Bench Waveform of Virtex II Pro

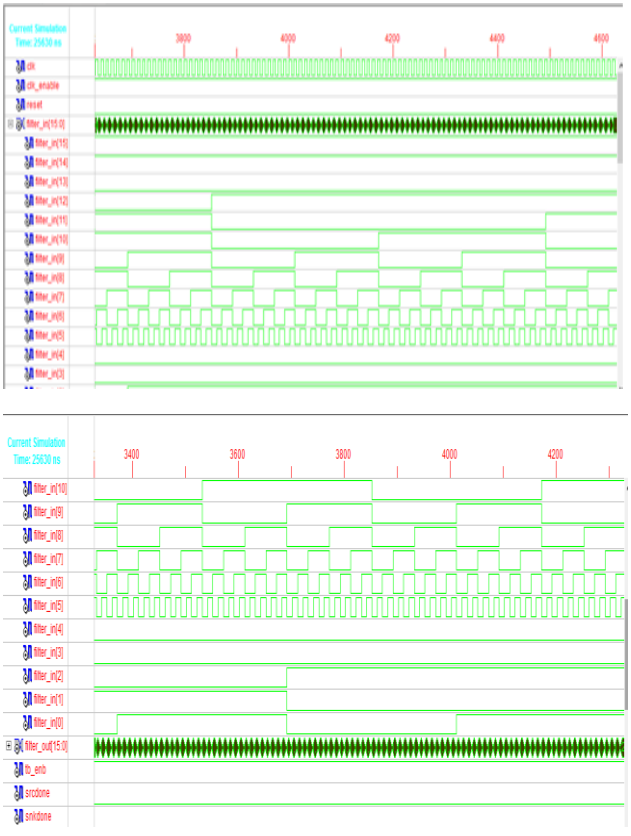

Fig 9. Test Bench Waveform of Spartan 3E

Table 1. Resource usage of SPARTAN 3E (3s500efg320-4)

FILTER STRUCTURE		Direct Form-I	Direct Form-II
S.No.	Logic Details	Used/Available	Used/Available
1.	Numbers of Slices	2678/4656	2443/4656
2.	Numbers of Flip-flops	657/9312	352/9312
3.	Numbers of LUTS	4567/9312	4356/9312
4.	Number of I/O bonds	35/232	35/232
5.	Numbers of Multipliers	20/20	20/20
6.	Speed in MHz	4.326 MHz	3.867 MHz

Table 2. Resource usage of VIRTEX II Pro (2vp30ff1152-5)

FILTER STRUCTURE		Direct Form-I	Direct Form-II
Sr No.	Logic Details	Used/Available	Used/Available
1.	Numbers of Slices	1054/13696	1066/13696
2.	Numbers of Flip-flops	657/27392	352/27392
3.	Numbers of LUTS	1530/27392	1815/27392
4.	Numbers of Multipliers	40/136	40/136
5.	Number of I/O bonds	35/644	35/644
6.	Speed in MHz	5.049 MHz	4.603 MHz

The Spartan-3E FPGA is the world's lowest cost logic device having system gates range from 100K to 1.6M gates and 66 to 376 I/Os range, 32 bit RISC soft processors & 18x18 multipliers that deliver upto 330 billion MACs per second .[9]On the other side Virtex Pro is the only FPGAs in the electronic industry that offered integrated PowerPc embedded technology & 3.12 Gbps serial transciver. It conist 30,816 logic cells and 136 -18 bit multipliers [10]. The comparsion of utilization summaries of both devices is shown in the form of table below-

Table 3. Resource utilization and speed comparison with Direct Form-I & II

FILTER STRUCTURE		Direct Form-I		Direct Form-II	
S.N	Logic Details	Spartan 3E	Virtex-II PRO	Spartan 3E	Virtex-II PRO
1.	No. of Slices	2678	1054	2443	1066
2.	No. of Flip-flops	657	657	352	352
3.	No. of LUTS	4567	1530	4356	1815
4.	No. of Multipliers	20	40	20	40
5.	Number of Bonded IOBs	35	35	35	35
6.	Speed in MHz	4.326 MHz	5.049 MHz	3.867 MHz	4.603 MHz

Table 1 shows the resource utilization by Spartan-3E for Direct-Form I and Direct-Form II IIR filter structure, Table 2 shows the resource utilization by Virtex 2P for Direct-Form I and Direct-Form II , Table 3 shows the resource utilization on Direct-Form I and Direct-Form II structure on both the devices.

Table 4. Percentage Resource utilization

FPGA DEVICE USED		Spartan 3E		Virtex 2P	
S.N	Logic Details	Direct Form	Direct-Form Symmetric	Direct Form	Direct-Form Symmetric
1.	No. of Slices	57%	52%	7%	7%
2.	No. of Flip-flops	7%	3%	2%	1%
3.	No. of LUTS	49%	46%	5%	6%
4.	No. of Multipliers	100%	100%	29%	29%
5.	Number of Bonded IOBs	15%	15%	5%	5%

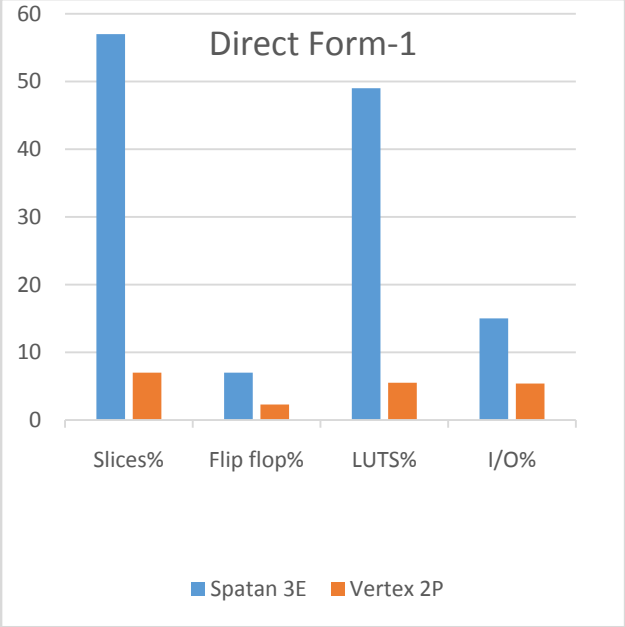

Fig. 10 Graphical representation of device utilization on Direct form-I IIR structure

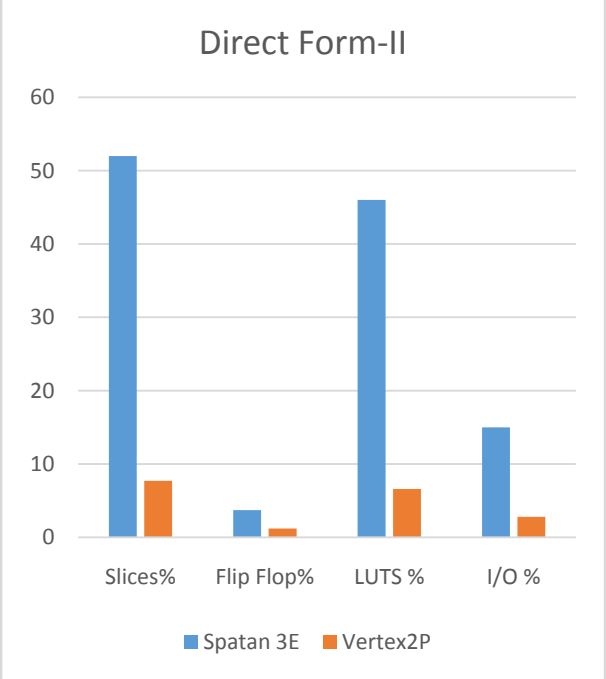

Fig. 11 Graphical representation of device utilization on Direct form-I IIR structure

5. CONCLUSION

In this paper the simulated VHDL model has been synthesized using Xilinx synthesized tool (ISE) on Spartan-3E (3s500efg320-4) and Virtex II Pro (2vp30ff1152-5) target FPGA device. Here, implementation of direct form-I & direct form-II structure on ISE is shown of IIR filter. That shows Virtex II Pro is 16.7% faster than Spartan-3E in direct form-I and 19.03% faster in direct form-II. So I considered direct form-I that gives better speed and better utilization of resource. The maximum delay in Spartan-3E is 231.144ns with 2443 numbers of slices, 20 numbers of multipliers and maximum delay in Virtex II Pro is 258.594ns with 1066 number of slices and 40 number of multipliers. In Vertex2p based device number of slices are less as compared to Spartan 3E based device.

For enhancing the speed and area consumption, MAC based parallel IIR filter has been presented. This MAC algorithm will take the advantage of look up tables and embedded DSP slices of target FPGA's.

6. REFERENCES

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7. AUTHOR PROFILE

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Chandni received her B.E. degree in Electronics and Communication Engineering from the Himachal Pradesh University in 2010, and M.E. degree in ECE Engineering from Punjab University in 2013. In 2013, she joined the Department of Electronics and Communication Engineering of Baddi University, as an Assistant Professor. She was the Convener of the National Conference on Recent Innovations in Electronics, Electrical and Computer Engineering held in Baddi University, Himachal Pradesh. In December 2015 she enrolled for PhD. in National Institute of Technical Teachers's Training & Research, Chandigarh. Her current research interests include VLSI Design, Digital Signal Processing, Nanoelectronic Devices.