FPGA based Asynchronous FIR Filter Design for ECG Signal Processing

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ABSTRACT
In this paper, Asynchronous FIR filter is designed and implemented for ECG signal processing. The use of asynchronous design approaches to construct digital signal processing (DSP) systems is a rapidly growing research area driven by a wide range of emerging energy constrained applications such as wireless sensor network, portable medical devices and brain implants. This inherent advantage of asynchronous design over conventional synchronous circuits allows them to be energy efficient. The technique used for the design and implementation is modified pipelining representation. This paper describes the analyzing and modelling of asynchronous design FIR equiripple filter using MATLAB, simulated with ISE and then implemented on FPGA devices. The proposed Asynchronous design FIR equiripple filter is implemented on two FPGA devices Xilinx's Spartan-3E, xc3s500e-4fg320 and Virtex 2P, 2vp30ff1152-5 and compared on the basis of Asynchronous FIR and Synchronous FIR filter for hardware resource utilization as well as speed. The hardware result shows that the proposed asynchronous designed on Virtex 2P is 10.72% faster than that designed on synchronous FIR filter on given specifications. The designed FIR filter on FPGA device Virtex 2P shows efficient area utilization as well as better speed as compared to that designed with synchronous FIR filter.

Keywords
Asynchronous FIR Filter, ECG, Filter, MATLAB, Xilinx.

1. INTRODUCTION
Digital signal processing is all about digital representations of the signal to analyze the signal and to extract the results after modification of signal. During processing of the signal, noise and interference due to variation of temperature affects the input signal. To restore the signal in its original form various filters are used with its architecture design. The two major types of Digital filters are Finite impulse response (FIR) and Infinite impulse response (IIR).

Asynchronous circuits are the circuits which are not governed by a Clock circuit or clock signal. Most digital circuits are fabricated on synchronous circuits due to their two advantages. One is all signals are binary and second all components share common clock. Asynchronous circuits employ handshake protocols to communicate with their environment, sequence operations and co-ordinate signals transfer within the circuit [1].

Asynchronous circuits also consist of many interesting properties over synchronous circuits namely: low electromagnetic noise emission, robustness for variations in supply voltage, fabrication process parameters, improved performance and temperature [1]. The use of asynchronous circuits in digital signal processing [DSP] is a growing area of research driven by a range of emergency energy applications such as wireless sensor networks, portable medical devices and biomedical applications. All these signals parameters vary smoothly and not change for long period of time. This feature of such signals make asynchronous circuits design better [3].

This paper describes the designing of Asynchronous architecture based FIR low pass digital filter for reducing noise in the ECG. The further contribution is inclusion of MATLAB program and analysis MATLAB program on FIELD PROGRAMMABLE LOGIC ARRAY (FPGA).Rest of the paper is organized as follows. In section II Related Technology and in section III the Overall Design of asynchronous architecture is presented. In section IV Experimental results is shown and in section V Results and comparison is discussed. Finally in section VI, conclusion is drawn.

2. RELATED TECHNOLOGY
A. Basic Finite impulse response (FIR) Filter
In signal response, FIR is a filter whose impulse response is of finite duration; because of its zero finite duration of time. To calculate the Transfer function of FIR filter having length-N can be calculated by:

$$y(n) = \sum_{k=0}^{M-1} h(k)x(n-k)$$

$$H(z) = \frac{Y(z)}{X(z)} = \frac{\sum_{k=0}^{n} b_k z^{-k}}{1 + \sum_{k=1}^{N} a_{kz^{-k}}}$$

…… .(1)

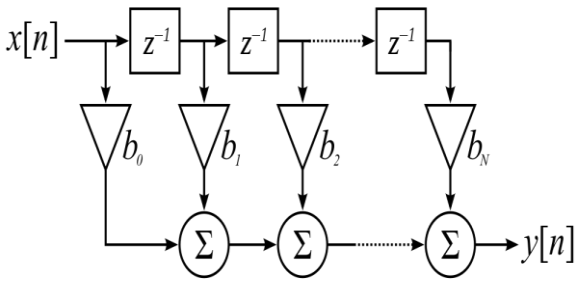

Fig. 1: Direct Form FIR Filter

Table 1 Various Windows Techniques

Window function	Attenuation of the first side lobe relative to major lobe /dB	Wide of main lobe	Attenuation of stop band minimum /dB
Hanning	-31	8π/n	44
Hamming	-41	8π/n	53
Blackman	-57	12π/n	74
Kaiser	Adjustable	Adjustable	Adjustable

3. THE OVERALL DESIGN

A. Asynchronous Architecture Based FIR Filter.

This filter design is based on the synchronous design as shown in figure 2. In order to replace synchronous design with asynchronous design the clocked registers is replaced by delay elements. In asynchronous circuits, communications is done by handshake protocols such as REQ, ACK, and Latch [5]. The basic operation of architecture is, when the senders send any data at the time of transmission the Request signal goes high. The receiver latches the new data and send acknowledge signal back to sender and request goes reset as shown in figure 3.

These asynchronous architecture components act as power adaptive processor scale which removes the token occupancy and increase the speed of the circuit. It also controls the token to propagating down to the next stage. The token from each stage is allowed to pass to the next stage only after when the global request goes high. There is also transfer of acknowledgement signal to each stage after global acknowledgement [4, 5].

The four cases of handshaking in Asynchronous design as:

CASE1: The sender sets Req. signal is high after date is sent and simultaneously global request signal is also become high.

CASE 2: The receiver receives the signal and send back ACK signal while Req. signal is still high.

CASE 3: The sender receives the ACK signal and reset the Req. signal only after resetting the global request signal.

The receiver reset the ACK signal after global request signal become low [6].

B. Asynchronous Design Multiplier

Asynchronous micro pipeline designs consist of much advantage over synchronous design in terms of its applications. Asynchronous and synchronous designs consist of adders for their designing circuits. While designing the circuits the number of transistors used in synchronous circuits is about 6000 and in asynchronous circuits is about 9000 transistors [5].

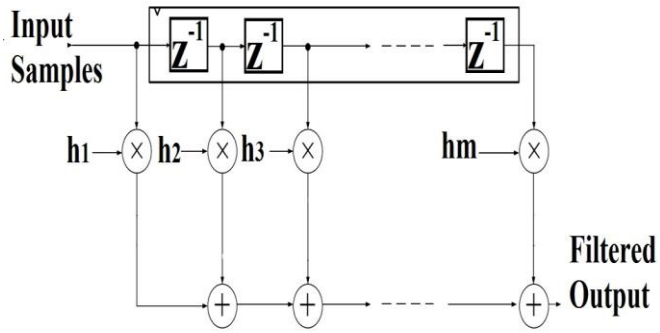

Fig. 2: Structure of FIR FILTER

While discussing about the speed, asynchronous circuits are much better than the synchronous circuits. The speed of synchronous circuits is only 20MHz and the speed of asynchronous circuits is 250MHz. The response time of synchronous circuits is about 800ns and the response time of asynchronous circuits is about 72ns which make asynchronous circuits much better than synchronous circuits [5, 6].

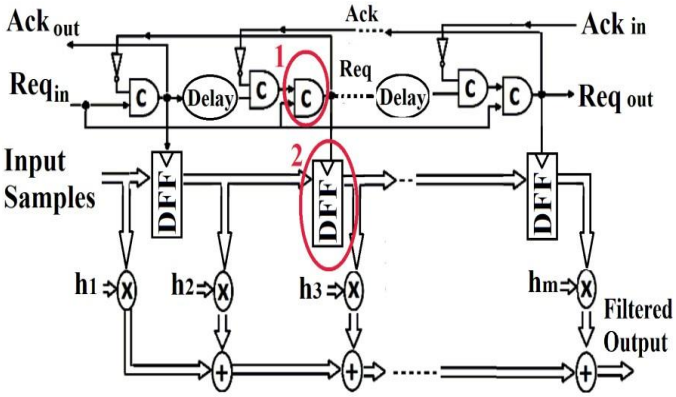

Fig. 3: Asynchronous Design Architecture

The response time between the input and output in synchronous design FIR pipelined filter is about 3.2µs and for asynchronous circuits the response time is about 372ns. This parameter show that the response time of asynchronous pipelined FIR filter is much better than synchronous FIR filter.

The average power consumption utilized in synchronous pipelined FIR filter is about 1.363W and in asynchronous design circuits the average power consumption is 1.953W [5,6].

C. Electrocardiography (ECG) Signal Generation

Electrocardiography (ECG) is the generalize process of recording the electrical activity of the heart over a period of time using the method of electrodes placed on the skin. These electrodes detect the electrical changes on the skin that arise from the heart muscles [7, 8].

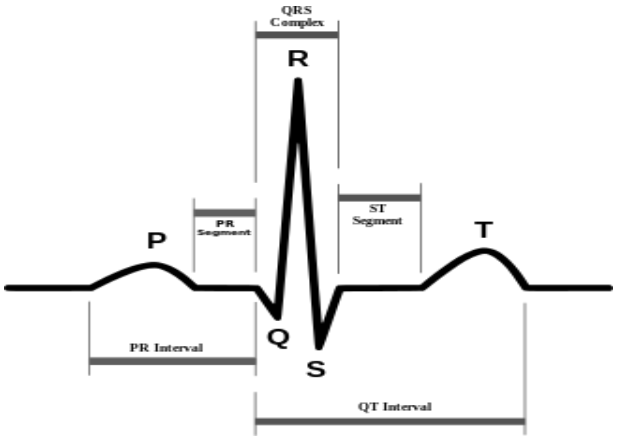

Fig. 4: ECG Signal

During receving the ECG signal from the heart muscles the noise or interference affect the output of the signal and causes false output is generated at the output. ECG signal is used as an important clinical tool for analyzing the activities of heart.

Normally ECG machine generate four types of wave at the output of the graph P, Q, R, S, T and U. Bio medically these wave are represented as P wave, QRS wave, T wave and U wave as shown in figure 4 [8].

4. THE EXPERIMENTAL RESULTS

A. Design and Simulation

To evaluate the proposed architecture, a low pass equiripple FIR filter has been considered the design specifications for filter shown below.

The sampling frequency range is about 125Hz.

The pass band frequency for low pass filter is about 35Hz.

The stop band frequency of low pass filter is 45Hz.

The pass band ripple is about 1db

The stop band ripple is about 80db.

This work has used MATLAB tool for designing electrocardiogram with reduced noise. The latter is used to develop two hardware implementations of the filter, one using conventional synchronous structure and the second is based on the proposed asynchronous filter architecture. Both filters are implemented on Xilinx synthesizer tool(XST). Here SPARTAN 3E 3s500efg320-4 family and VIRTEX 2vp30ff1152-5 family is used

The magnitude plot is shown in figure. 5. This plot gives the constant output with high stop band attenuation.

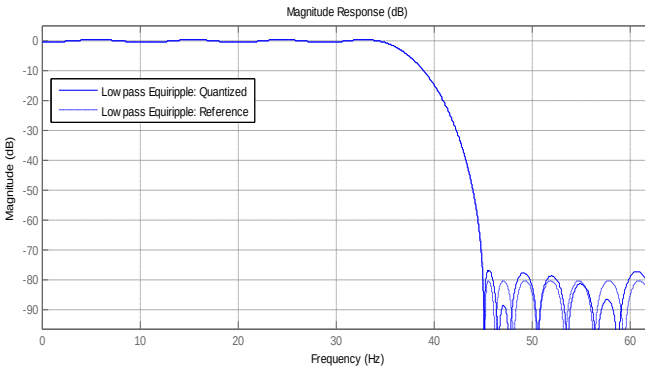

Fig. 5: Magnitude Plot

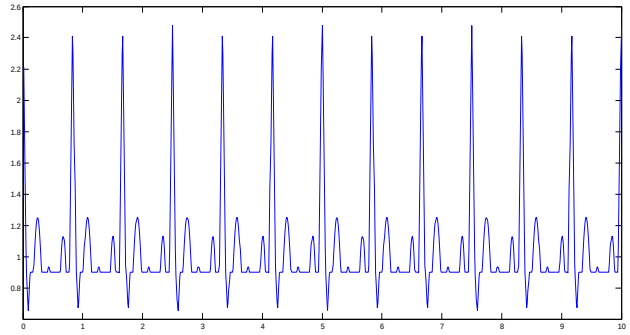

Fig. 6: ECG Signal

The ECG signal is shown in figure 6. This signal defines that there is no noise present in the signal.

The input signal during transmission is affected by the unwanted signal such as noise, interference and the resultant output of ECG signal is not clear as shown in figure 7.

The unwanted signal is generatd by the interference generated from the heart muscles, skin and due to variation in the electrical activity. All these activity is recorded by the electrodes and mix with the input signal.

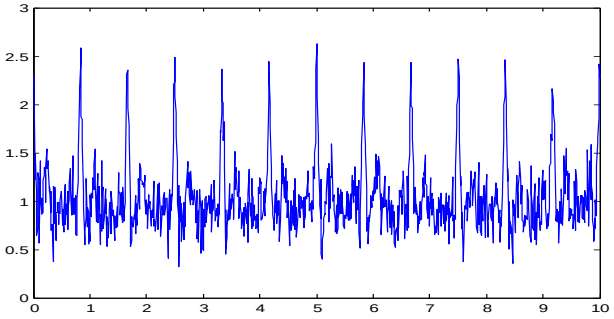

Fig. 7: Noisy ECG signal

CASE 1: Corrupted ECG signal is tansmitted through asynchronous design based low pass FIR filter. The output is shown in figure 8.

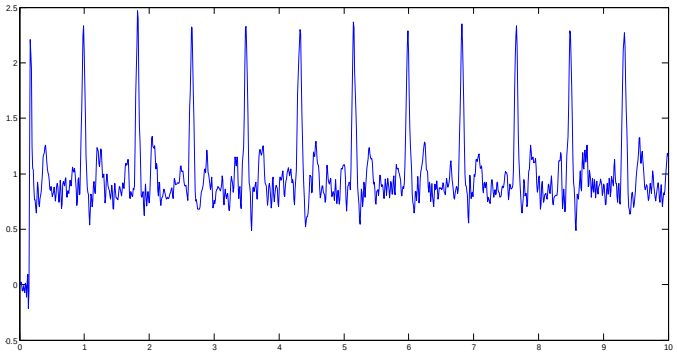

Fig. 8: Asyncronous FIR Filtered ECG signal

CASE 2: Corrupted ECG signal is tansmitted through Synchronous design based low pass FIR filter. The output is shown in figure 9.

By comparing the output of asychronous architecture and sychronous architecture, it shows that output of asychronous architecture give much better output as compared to synchronous architecture based FIR filter

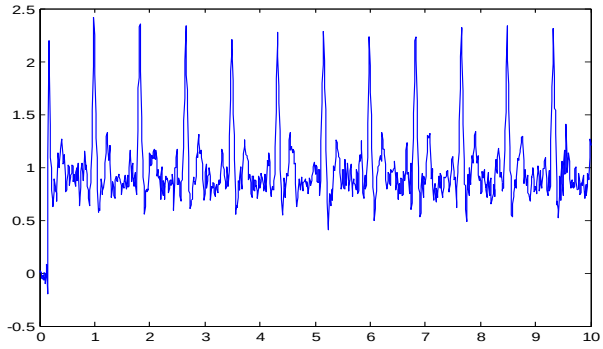

Fig. 9: Syncronous FIR Filtered ECG signal

5. RESULTS AND COMPARISON

A. FPGA Hardware Result Analysis

Field Programmable Gate Arrays (FPGA) can be reprogrammed as many times in order to achieve the desired results. The use of FPGAs in the design process and implementations provide more design flexibility, and reducing a cost and developing time [8, 9].

Developed VHDL code has been synthesized using Xilinx synthesizer tool (XST) and implemented on Spartan3E 3s500efg320-4 and VIRTEX 2vp30ff1152-5 family. To observe the speed and resource utilization the developed FIR filter is designed on SPARTAN 3E and VIRTEX 2P shown in the Table II and Table III.

Table II Resource Usage Of Spartan-3e (3s500efg320-4)

Sr. No.	Logic Details	Used/ Available	Utilization (%)
1.	Number of Slices	1370/4656	29%
2.	Number of slices Flip Flops	528/9312	5%
3.	Number of 4 input LUTs	2030/9312	21%
4.	Number of bonded IOBs	35/232	15%
6.	Max frequency	12.199MHz	-
7.	Min. period	81.975ns	-
8.	Number of GCLKs	1/24	4%

Table III Resource Usage Of Virtex 2p (2vp30ff1152-5)

Sr. No.	Logic Details	Used/ Available	Utilization (%)
1.	Number of Slices	794/13696	5%
2.	Number of slices Flip Flops	528/27392	1%
3.	Number of 4 input LUTs	976/27392	3%
4.	Number of bonded IOBs	35/644	5%
6.	Max frequency	13.295MHz	-
7.	Min. period	76.368ns	-
8.	Number of GCLKs	1/16	6%

Table IV shows the speed and resource utilization by Spartan-3E for asynchronous and synchronous FIR filter design, Table V shows the speed and resource utilization by Virtex 2P for asynchronous and synchronous FIR filter design.

B. Comparison Between Asynchronous And Synchronous FIR filter design

Table IV Resource Utilization And Speed By Spartan-3e (3s500efg320-4)

Sr. No.	Logic Details	Asynchronous	Synchronous
1.	Number of Slices	1370/4656	1380/4656
2.	Max frequency	12.199MHz	11.089MHz
3.	Min. period	81.97ns	82.138ns

Table V Resource Utilization And Speed By Virtex 2p (2vp30ff1152-5)

Sr. No.	Logic Details	Asynchronous	Synchronous
1.	Number of Slices	794/13696	793/13696
2.	Max frequency	13.295MHz	12.007MHz
3.	Min. period	76.368ns	76.411ns

C. Simulation

Test bench waveform through behavioural model of ISE Simulator using Spartan-3E & Virtex 2P is shown in Fig. 10 and Fig. 11.

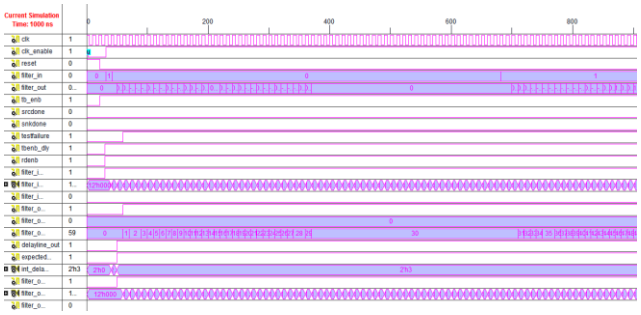

Fig. 10: SPARTAN 3E 3s500efg320-4 simulations

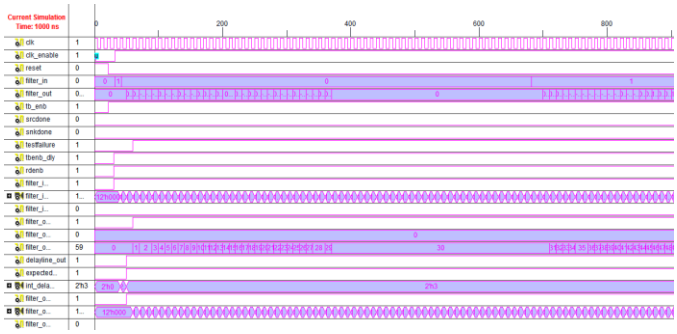

Fig. 11: VIRTEX 2vp30ff1152-5 simulations

6. CONCLUSION

In this paper the simulated VHDL model has been synthesized using Xilinx synthesized tool (ISE) on Spartan-3E (3s500efg320-4) and Virtex 2P (2vp30ff1152-5) target FPGA device. Here, implementation of Asynchronous & synchronous FIR design on ISE is shown for ECG signal processing. This shows Asynchronous design is 10.72% faster than synchronous design in Virtex 2P and 10.01% faster in Spartan-3E. So Asynchronous FIR filter is considered that gives better speed and better utilization of resources. The maximum delay in Spartan-3E is 81.975ns with number of slices to be 528, whereas maximum delay in Virtex 2P is 76.368ns with same numbers of resources. Hence it can be concluded that Virtex 2P in asynchronous design FIR filter is the best choice for better results in terms of speed, timing analysis and resources.

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8. AUTOR PROFILE

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Chandni received her B.E. degree in Electronics and Communication Engineering from the Himachal Pradesh University in 2010, and M.E. degree in ECE Engineering from Punjab University in 2013. In 2013, she joined the Department of Electronics and Communication Engineering of Baddi University, as an Assistant Professor. She was the Convener of the National Conference on Recent Innovations in Electronics, Electrical and Computer Engineering held in Baddi University, Himachal Pradesh. In December 2015 she enrolled for PhD. in National Institute of Technical Teacher's Training & Research, Chandigarh. Her current research interests include VLSI Design, Digital Signal Processing, and Nano electronic Devices.