A Novel 7T SRAM Cell Layout Design with Low Average Power in Read and Write Cycles

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ABSTRACT
The system memories requirement depends greatly on the nature of the applications which run on the system. Memory performance and capacity requirements are small for simple, low cost systems. In contrast, memory throughput can be the most critical requirement in complex, high performance systems. The following general types of memories can be used in systems such as Volatile and non-volatile memories. SRAM can be found in the cache memory of a computer or as a part of the RAM digital to analog converters on video cards. Static RAM is also used for high-speed registers, caches and small memory banks like a frame buffer on a display adapter. Several scientific and industrial subsystems, modern appliances, automotive electronics, electronic toys, mobile phones, synthesizers and digital cameras also use SRAM. It is also highly recommended for use in PCs, peripheral equipment, printers, LCD screens, hard disk buffers etc. Different transistor counts in used in SRAM architecture such as Bipolar junction transistors used in TTL and ECL which is very fast but consumes a lot of power and MOSFET used in CMOS which is used at low power and also very common today. This paper proposed to improve the stability of SRAM cell and also reduces the average power in standby mode. This paper presents a low average power based layout design of 7T SRAM [1] architecture.

Keywords
SRAM, Average power, Voltage Scaling, MOSFET, Flip flop, NMOS, PMOS, CMOS.

1. INTRODUCTION
There are two key features to SRAM - Static random Access Memory, and these set it out against other types of memory that are available:

1. **The data is held statically:** This means that the data is held in the semiconductor memory without the need to be refreshed as long as the power is applied to the memory.
2. **SRAM is a form of random access memory:** A random access memory is one in which the locations in the semiconductor memory can be written to or read from in any order, regardless of the last memory location that was accessed.

The circuit for an individual SRAM memory cell comprises typically two or four transistors. In this format the circuit has two stable states, and these equate to the logical "0" and "1" states. These additional transistors are used for functions such as implementing additional ports in a register file, etc for the SRAM memory. Simple Operational Concept of SRAM cell shown in fig1-

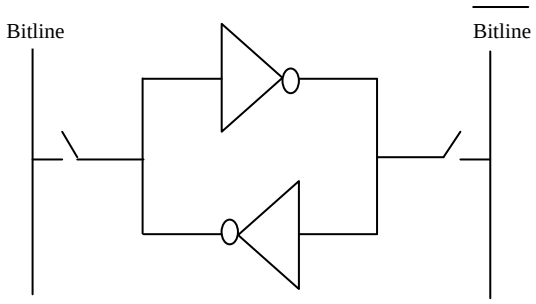

Fig 1: simple line diagram of SRAM cell Operational Concept

As shown in the above figure the inverters are connected back to back to form latch. These are connected by bit line. Access transistors are connected between bit line and invertors to read or write the data.

Although any three terminal switch device can be used in an SRAM, MOSFETs and in particular CMOS technology is normally used to ensure that very low levels of power consumption are achieved. With semiconductor memories extending to very large dimensions, each cell must achieve very low levels of power consumption to ensure that the overall chip does not dissipate too much power. Power reduction can be achieved by various methods like, dual threshold based operation of SRAM circuit [2], by using a modified architecture that reduces the power in data write [3] operation or data read operation, etc.

1.1 Design of SRAM 6T Architecture-
The standard cell consist of six transistor, as shown in fig 2 the nMOS access transistors (A1 and A2) located at the ends of circuit and a pair of cross-coupled inverters comprise of memory cell. The nMOS element (D1 and D2) of the latch are the driver transistors, while pMOS (P1 and P2) are the pull-up transistors. The access transistor operates when the word line is raised, for read or writes operation, connecting the cell to the bit lines (Bit line, ~Bit line). The cell has three different operation modes. In the standby state, word line is not asserted, so access transistors are turned off. Therefore, cell cannot be accessed and two cross-coupled inverters will continue to feed back each other, as long as they are connected to the supply, and data will hold in the latch. The read operation starts by pre-charging the bit lines high, then allowing them to float. Afterwards, word line is asserted, turning on all access transistors.

The data stored in the nodes are driven onto bit lines. A voltage difference is developed between bit lines and a sense amplifier detects the value of the cell.

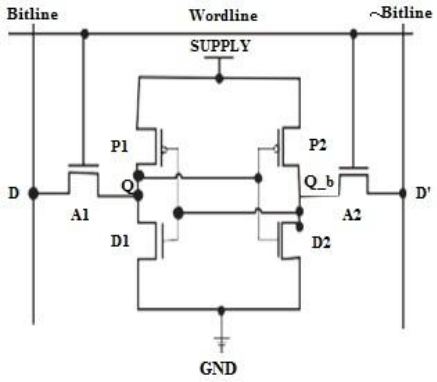

Fig 2: The standard 6T SRAM cell architecture

During the write operation, the bit lines are driven to complementary voltage levels and then word line is raised. The data to be written into the cell are driven onto the bit lines and one of the storage nodes is discharged through the access transistor. The cross-coupled inverters raise the voltage on the opposite storage node and latch the cell. Thus, the new data overpowers the cross-coupled inverters. The central challenges in SRAM design are minimizing its size and ensuring that the circuitry holding the state is weak enough to be overpowered during a write cycle (write ability), yet strong enough not to be disturbed during a read cycle (read stability).

To read a "D=0"

- When the wordline at 0V, both access transistors are off.
- Pre-charge both bit lines high then the wordline will go high.
- If a "D=0 D=1" is stored, then Wordline is High causes A1 to pass 0V to D2/P2, VDD to D1/P2
- Charge flow P2≥A2, thus charging the B bit line voltage.
- Charge flow A1≥D1, thus discharging the B bit line voltage.

To read a "D=1"

- Wordline at 0V, both access transistors are off .
- Pre-charge both bit lines high VDD then the wordline will go high.
- If a "D=1 D=0" is stored, then Wordline=High causes A1 to pass VDD to D2/P2, 0V to D1/P1
- Charge flow A2≥D2, thus discharging the B bit line voltage.
- Charge flow P2≥A1, thus charging the B bit line voltage.

To write a "1", initially at a "0"

- Wordline at 0V, both access transistors are off
- Pre-charge one bit line high (D=B=VDD), the other low (D=B=0V) then the wordline will go high.
- Source (B) of A1 goes to 0≥VDD-Vt, and drain (B) of A2 goes to VDD≥0V.
- Positive feedback takes over, and cell stores a "1" on D

To write a "0", initially at a "1"

- Wordline at 0V, both access transistors are off
- Pre-charge one bit line high (B=VDD), the other to ground (B=0V) then the wordline will go high.
- Source (B) of A1 goes to VDD≥0V, and drain (B) of A2 goes to 0≥ (VDD-Vt)
- Positive feedback takes over, and cell stores a "0" on D.

1.2 Design of 7T- SRAM

This section describes 7T SRAM cell design. A comparative study of a novel 7T cell design with the conventional design in [4] shows a performance improvement of novel 7T-SRAM designs. Using CMOS technology the design is implemented in 180nm.The main aim of this 7T SRAM cell is to reduce the consumption of leakage power and improve the stability of the memory cell in normal region of operation. Some design architecture used CMOS transistor operation in sub-threshold region [5] for reducing power. A modified 8-T design architecture is proposed [6] for low power and low voltage circuits.

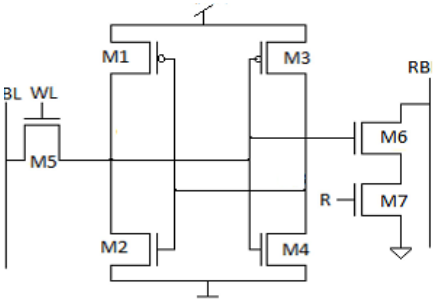

Fig 3: schematic of proposed SRAM cell

As shown in fig 3 the arrangement of the 7T SRAM cell circuit, the two inverters (M1, M2 and M3, M4) are connected cross M5 which is a write access transistor and two M6 and M7 transistor are stacked with read signal for the read operation. RBL used for read bitline and WBL used for write bitline operation. An improved read stability based asymetric design of SRAM [7] shows that selective threshold voltage control is more effective than adjusting transistor size for read stability.

In standby mode of operation, the proposed output node of SRAM cell maintains to store data until the power is available from the power supply. To solve the problem there are two techniques first is the supply of voltage is decreased and in second the voltage of GND node is increased and across the SRAM cell the effective voltage is decreased.

1.2.1 Write-1 operation-

In the write operation mode in the SRAM Cell the bit line WBL is used to write the data. To perform the write operation EBL and WL line are used. In the operation when we write '1' in the cell the WBL is charged to VDD and M5 enable the WL signal and then the 'Q' node start charging and turns to M4 leads to flip 'QB' node to logic '0'. Then 'QB' node helps enabling the M1 for writing logic' 1 ' at 'Q' node.

1.2.2 Write-0 operation-

If data need to be written is '0', write bit-line should be at logic low, and M5 turns on, by enabling WL signal. Then the node 'Q' starts discharging and turns on M3 which in turn flips 'QB' node to logic '1'. After that 'QB' helps turning M2 on, which facilitates discharging 'Q' node properly, and consequently logic '0' is obtained at 'Q' node.

1.2.3 Read 0 or 1 operation-

In Read operation the SRAM data is read from the cell. At the initial stage the data in the bit line is begun pre-charging to VDD. After pre-charging the bit line the read signal is activated. It depends on whether the data in RBL holds or discharged is decided by SRAM cell. After pulling the read line to VDD RBL is discharged, then it going to indicate the SRAM cell store '0' in it. If it hold the charge then it store '1'. Then read operation WL is inactive at logic '0'.

2. SIMULATION RESULT

2.1 Layout of 6T SRAM-

The proposed layout design of 6T SRAM performed at 180 nm technology on microwind shown in fig 4-

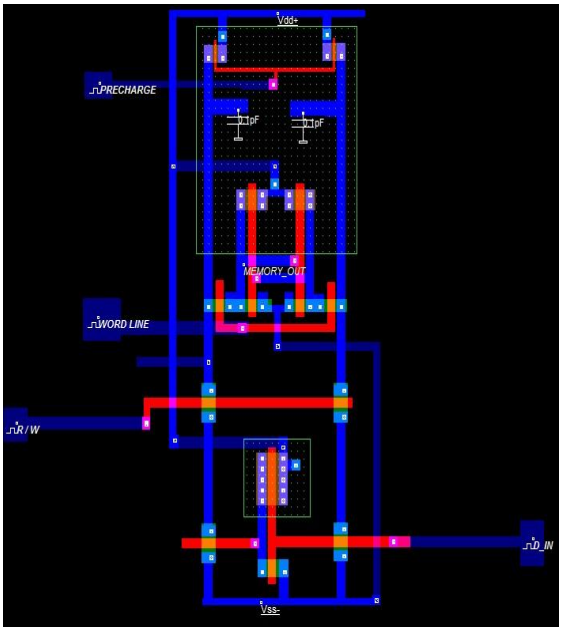

Fig 4: Proposed 6T SRAM layout design

2.2 Layout of 7T SRAM-

The proposed layout design of 6T SRAM performed at 180 nm technology on microwind shown in fig 5-

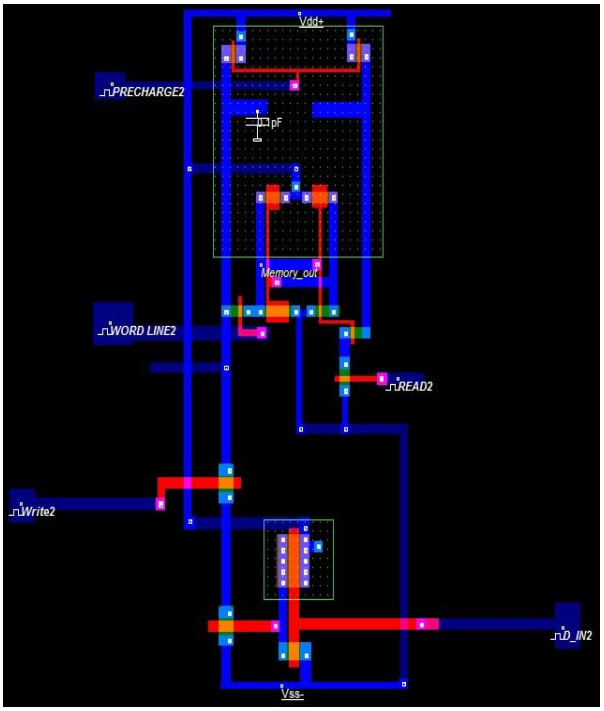

Fig 5: Proposed 7T SRAM Layout Design

2.3 Wave simulation of 6T and 7T SRAM-

Fig 6 shows the proposed waveform of 6T SRAM design simulation for read and write operations. However the read and write delay is almost same in the proposed design. Fig 7 shows the proposed waveform of 7T SRAM design simulation for read and writes operations. However the read and write delay is almost same in the proposed design.

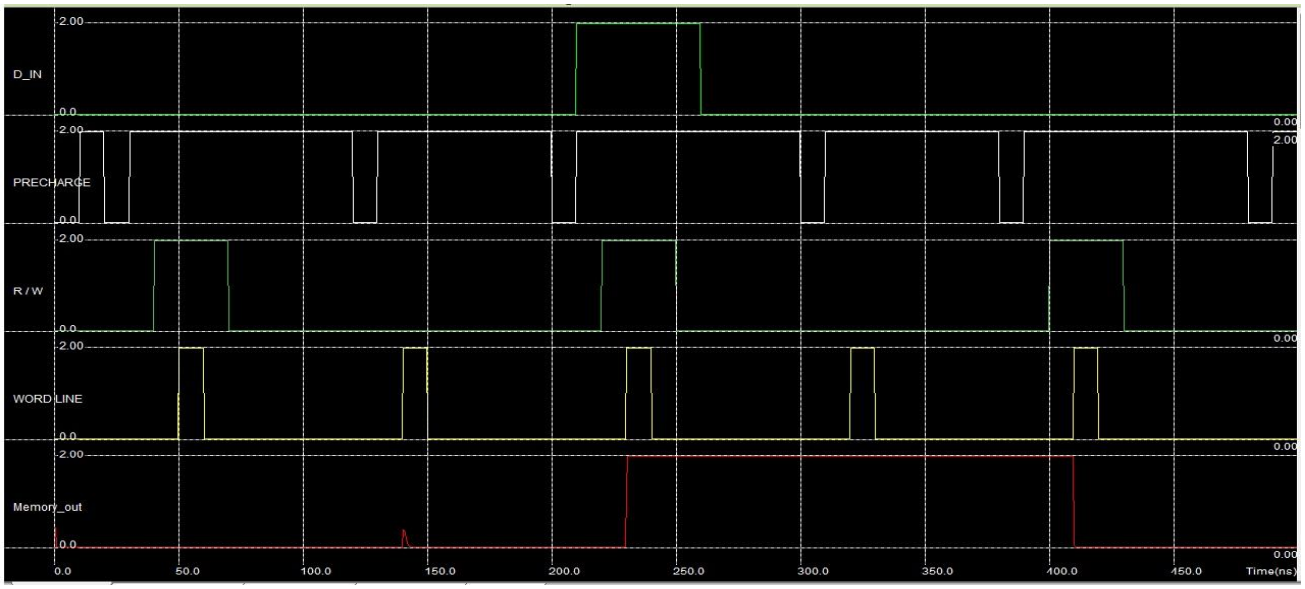

Fig 6: 6T SRAM proposed waveform

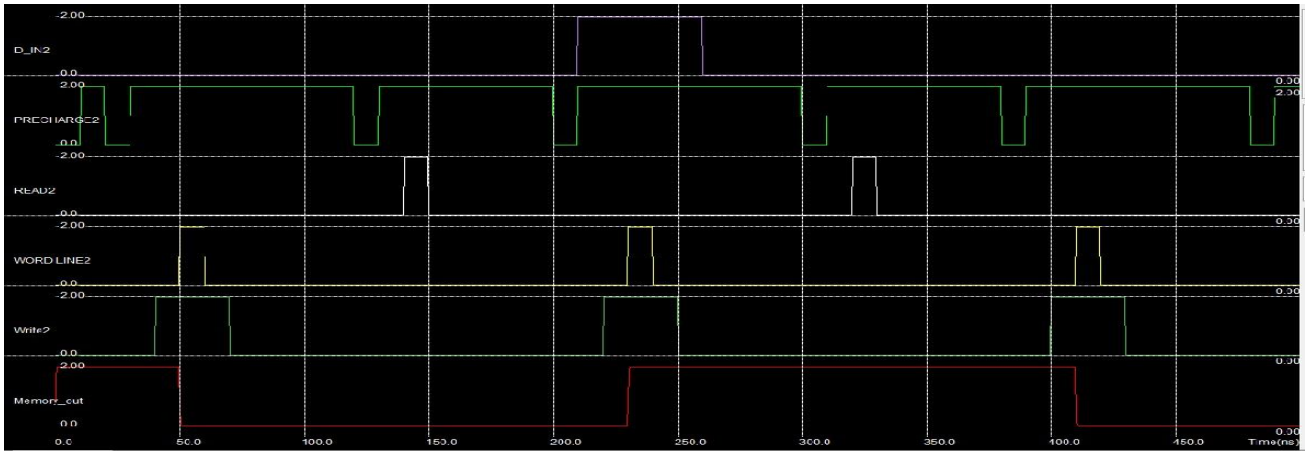

Fig 7: 7T proposed waveform

2.4 Average Power comparison of SRAM cells-

It is observed that the average power dissipation shown in table below shows the amount of power is very much less as compared with 7T SRAM to the conventional 6T SRAM in read as well as write mode operation using 180nm and 45nm technology. Table shows the adiabatic operation of the circuit gives the reduction of the average power dissipation.

Table I- Average power dissipation (µW) of SRAM cell in read and write operations

	6T-SRAM	7T-SRAM
180nm		
[1]	4.690	1.593
Proposed	3.107	1.514
45nm		
[1]	0.457	0.240
Proposed	0.114	0.057

2.5 Average power comparison chart-

Various low power design architectures are already proposed by scholars for SRAM cell based on popular approaches like data retention gated ground [8], dynamic threshold voltage, etc. In the present work power reduction is achieved using asymmetric 7T SRAM architecture. The graph in fig 8 and fig 9 shows the delay when compared with the proposed 7T SRAM cell to conventional 6T SRAM cell.

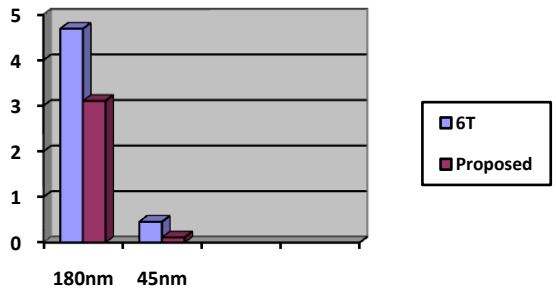

Fig 8: Average Power comparison with the proposed 6T SRAM cell to conventional 6T SRAM cell

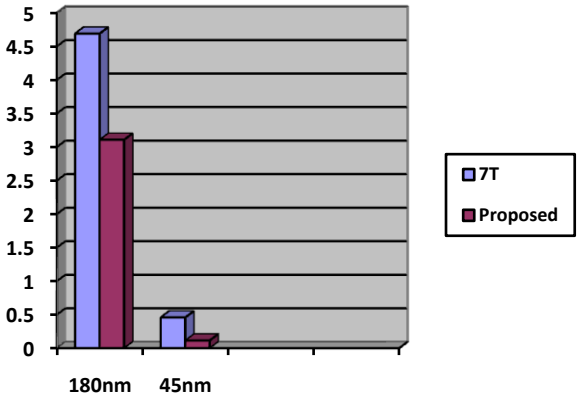

Fig 9: Average Power comparison with the proposed 6T SRAM cell conventional 7T SRAM cell

3. CONCLUSION AND FUTURE SCOPE

It is observed that the average power dissipation is much less as compared with 7T SRAM to the conventional 6T SRAM in read as well as write mode operation. The power consumption of novel 7T SRAM reduce the average power dissipation this increases the speed and power consumptions are good as compared to other SRAM cell. The proposed SRAM cell has been found to consume less power when it compared with conventional 6T SRAM.

In future, leakage current will play a vital role to reduced power consumption. Thus special techniques could be improved in future for these SRAM cells to achieve power reduction.

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5. REFERENCES

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