Abstract

This work describes a 12-bit pipeline ADC (Analog-to-Digital Converter) for CMOS (Complementary Metal Oxide Semiconductor) that is implemented in a TSMC 0.18μm CMOS process. The proposed ADC utilizes the Threshold Inverter Quantization (TIQ) technique that uses two cascaded CMOS inverters as a comparator. The TIQ flash ADC achieves high speed, small size, low power consumption, and low voltage operation compared to other ADCs. The sample and hold circuit have high sampling rate. This design is implemented and fabricated in TSMC 0.18μm CMOS verified on the LT SPICE in 0.18μm technology.

References

1. A 12-bit 20MS/s 56.3mW Pipelined ADC with Interpolation-Based Nonlinea Calibration Jie Yuan, Member, IEEE, Sheung Wai Fung, Kai Yin Chan, and Ruoyu Xu, Student Member, IEEE 2011
A Review on Pipe Line Analog to Digital Converter using 0.18µm CMOS Technology

Enríquez, D. Bisbal, M. Banu, and J. Barbolla IEEE 2004
3. [3 ] A 6 BIT 1.2 GSps low power flash ADC IN 0.13um digital CMOS Martin clara andreas santrer thamos hartig IEEE 2005
4. [4 ] A Pipeline Analogue to Digital Converter in 0.35 µm CMOS S.W. Ross†, Student Member, IEEE, and S. Sinha Member, IEEE 2007
5. A 7 bit 16MS/s low power cmos pipeline ADC Zhuang zhaodong ,li zhiqug IEEE 2011
11. Patrick Quinn, Maxim Pribytko ‘Capacitor Matching Insensitive 12-bit 3.3MS/s Algorhmic ADC in 0.25pm CMOS’
20. J.Li and U-K Moon ‘Background calibration Technique for multistage pipeline ADCs with digital redundancy,’ IEEE. J.of solid-state circuit,
21. Tingting Chen 1 heying Li2 Bo Li 3 Yuemei Li4 Chunlei Wang4 Jianjian Wang4 , ‘Improved power scaling issue for Pipeline ADC’, International

Index Terms

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Keywords
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