Abstract

Processor speed largely governed by the multiplier architectures. It is desired to have faster ALU with lower power consumption for portable applications to have good battery life. Hence, there is need to address different multiplier architectures. In this paper, the analysis of 4-bit multiplier using a Vedic Mathematics (Urdhva Tiryagbhyam sutra) and conventional multiplier with two different adders has been realized using carry look ahead adder and ripple carry adder. Comparative study of multipliers is done for low power requirement and high speed. The main purpose of the paper is to investigate the better adder and multiplication technique. It is observed that the conventional multiplier with CLA adder is more stable and power efficient. Conventional multiplier with CLA adder is having 117 % less energy delay product than Vedic with RCA adder, 62.0 % less than CLA based Vedic multiplier and 30.7 % less than conventional multiplier with RCA adder at supply voltage 0.9 V. Conventional multiplier with CLA adder is good over RCA adder based multiplier

References

Index Terms

Computer Science

Circuits and Systems
Keywords

Energy Delay Product (EDP); Ripple Carry Adder; Carry look ahead adder; Energy Delay Product (EDP)