Abstract

Devices optimization for power and speed is a major issue in ultra low power applications. The evolution of the MOSFET has proven to be the best choice for next generation processes. Portable device should have good battery life. Processor speed depends mainly on the multiplier. Paper present the analysis of 4-bit multiplier using a Vedic Mathematics (Urdhva Tiryaagbhyam sutra) and conventional multiplier with two different adders has been realized using carry look ahead adder and ripple carry adder. Comparative study of multipliers is done for low power requirement and high speed. The main purpose of the paper is to investigate the better adder and multiplication technique. It is observed that the conventional multiplier with Carry look ahead adder is stable and power efficient. Finfet based conventional multiplier with CLA adder is having 10 % less energy delay product than Finfet based VEDIC multiplier with CLA adder and 21.9 % less than FDSOI based conventional multiplier with CLA adder at supply voltage 0.9 V. The variation shows that Finfet based vedic multiplier with CLA adder is having less process variation than fdsoi based conventional multiplier with CLA adder.
References


Index Terms

Computer Science
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Keywords

Ripple Carry Adder; vedic multiplier; Energy Delay Product(EDP)