A Result Analysis of ASIC Design of Reversible Multiplier Circuit

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ABSTRACT
Reversible logic is very lots of in demand for the long term computing technologies as they are known to supply low power dissipation having its applications in Low Power, Quantum Computing, nanotechnology, and Optical Computing. during this paper, we have got given and implemented reversible Wallace signed multiplier circuit in ASIC through changed Baugh-Wooley approach using normal reversible logic gates/cells, based on complementary pass transistor logic and are valid with simulations, a layout vs. schematic check, and a design rule check.

Keywords
Reversible logic gates, Reversible logic circuits, Quantum Computing Systems, Wallace Signed multiplier, Baugh-Wooley approach.

1. INTRODUCTION
Reversible logic has attracted significance attention in recent years, leading to entirely different approaches like synthesis, optimization, simulation and verification. Power dissipation and therewith heat generation could be a major problem for today's laptop chips. The 30-year-long trend in electronics has been to increase each speed and density by scaling of device parts. Throughout this trend higher level of integration and new fabrication processes reduced the heat generation within the last decade. An additional basic reason for power dissipation arises from the observations made by Landauer already in 1961.

Quantum gates that are represented by unitary matrices have potentials to implement reversible logic circuits. Every Quantum gate represents a valid Quantum operation that should be unitary and hence should be reversible. That's Quantum gates are reversible, unlike several classical logic gates. Reversible logic gate/circuit may be defined as follows:

Definition 1: For an n input, m output gate, if there's a one-to-one correspondence between its inputs and outputs, and then this logic gate is reversible.

Definition 2: A gate is reversible if and as long as the (Boolean) perform is bijective i.e. a gate is reversible if it maps every input vector into a unique output vector and vice versa.

Definition 3: A garbage bit (G) is a further output, that aren't used or unwanted, that produces an n-input m-output performs reversible.

Definition 4: variety of ancillary inputs known as ancillary that are constant inputs that are won't to maintain the reversibility of the circuit.

Definition 5: Quantum cost (QC) of a gate is that the variety of elementary quantum operations that are used to implement the entire functionality. All elementary 1 x 1 and 2 x 2 qubit gates have quantum value of one

Definition 6: Flexibility refers to the universality of a reversible gate in realizing additional functions.

Definition 7: Delay for reversible circuits is that the maximum number of gates during a path from any input line to any output line. This definition relies on 2 assumptions 1) every gate performs computation in one unit time, and 2) all inputs to the circuit area unit on the market before the computation begins.

Reversible logic has received necessary attention in recent years as a results of it's impossible to construct quantum circuits whereas not reversible logic gates. An irreversible laptop can always be created reversible by having it save all the information it'd otherwise throw away. The concept of reversible computing depends on invertible primitives and composition rules that preserve invertibility. With these constraints, one can still satisfactorily affect every useful and structural aspects of computing processes; at an identical time, one attains a better correspondence between the behavior of computing systems and additionally the microscopic physical laws that underly any concrete implementation of such systems.

2. THEORY
A reversible logic circuit bought to have the following features:

• Use minimum variety of reversible gates.

• Use minimum variety of garbage outputs.

• Use minimum constant inputs.

Multiplication could be a heavily used arithmetic operation in several procedure units. It's necessary for the processors to have high speed multipliers. During this paper, a unique reversible multiplier circuit using reversible HNG gates is conferred. We tend to show that the planned reversible multiplier factor circuit is better than the present designs in term of variety of gates, variety of garbage outputs, variety of constant inputs and hardware complexness.

Reversible gate generates a permutation of input vectors. A k x k reversible gate uniquely maps k input vectors to k output vectors. There has one-to-one correspondence between them. A circuit is said to be reversible if the input vector may be uniquely determined from the output vector and there's a matched correspondence between its input and output assignments, i.e. not only the outputs may be uniquely determined from the inputs however additionally the inputs may be recovered from the outputs. Thus, the amount of

inputs and outputs in reversible logic circuits (gates) are equal. Such circuits (gates) permit the reproduction of the inputs from determined outputs and that we will recover the inputs from the outputs. In Reversible circuit, following parameters are calculated for comparison of various circuits.

Number of Gates (N): the amount of reversible gates used in circuit.

Number of Constant inputs (CI): This refers to the amount of inputs that are to be maintained constant at either zero or one so as to synthesize the given logical perform.

Number of Garbage Outputs (GO): This refers to the amount of unused outputs present during a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to realize reversibility.

Quantum value (QC): This refers to the value of the circuit in terms of the cost of a primitive gate. It's calculated knowing the quantity of primitive reversible logic gates (1x1 or 2x2) needed to realize the circuit.

The Design constrains for reversible gate are decreased higher than parameters and fan-out isn't allowed. During this paper, a 8x8 number using reversible gate is planned.

3. METHOD

3.1 Design of Reversible Wallace Sign Multiplier

To compute product of two signed numbers, we have used modified Wallace approach. Reversible multiplier design is divided into two parts: partial product generation circuit and then multi-operand addition circuit.

Reduction in range of partial product to be added is achieved by using Wallace tree multiplier. Reduction in range of addition in critical path is aimed using tree structure. Figure Below shows the architecture of 8x8 bit Wallace tree multiplier.

Wallace tree reduces the amount of partial product to be added into two final intermediate results. The Wallace tree basically multiplies 2 unsigned integers; A Wallace tree is an efficient hardware implementation of a digital circuit that multiplies 2 integers. The planned design aims to reduce the general latency. This results in increased speed and reduced power consumption. The planning makes use of compressors in place of full adders, and also the final carry propagate stage.

The Wallace tree construction technique is usually used to add the partial product during a tree-like fashion so as to provide 2 rows of partial product that may be added within the last stage. Though fast, since its critical path delay is proportional to the logarithm of the amount of bits within the multiplier, the Wallace tree introduces different issues like wasted layout space and increased complexness. Within the last stage, the two-row outputs of the tree are added using any high-speed adder like carry save adder to generate the output result.

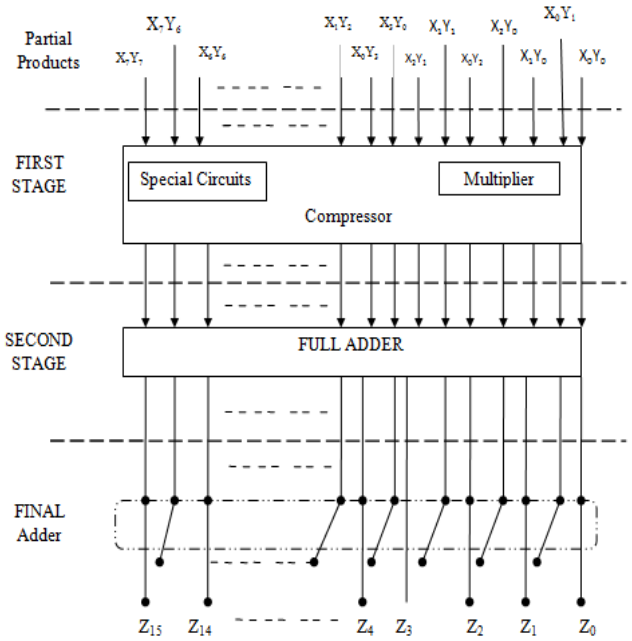

Fig.1 Wallace tree multiplier

3.1.1. Partial Product

Partial products multiplication is based on the distributive or grouping, property of multiplication. A person using this algorithm multiplies each digit of one factor by each of the digits in the other factor, taking into account the place value of each digit. Then the person adds all the partial products to find the total product (each partial product is either a multiplication fact or an extended multiplication fact). Partial product is a method of doing multiplication in math. The reason it's called "partial product" or "partial answer" (the word "product" means answer in multiplication just like "sum" means answer in addition) is because you are doing many "parts" of a larger multiplication. To get to the final answer, you must add up all "parts". The Feynman gate is used in the partial product.

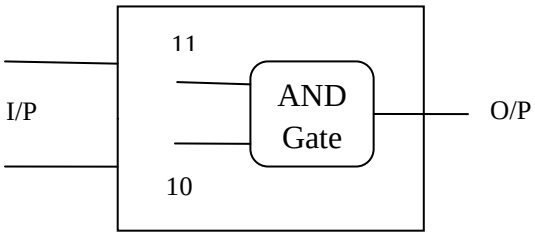

Fig. 2 Partial Product

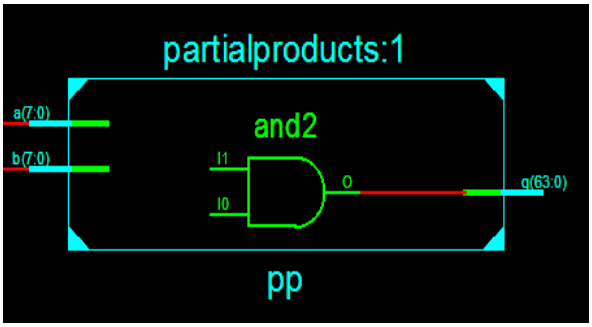

Fig.3 Schematic of Partial products

3.1.2. Full Adder

The Full Adder consists of XOR gate and AND gate. In this the three input and two output that is sum and carry. The Peres gate is used in the full adder.

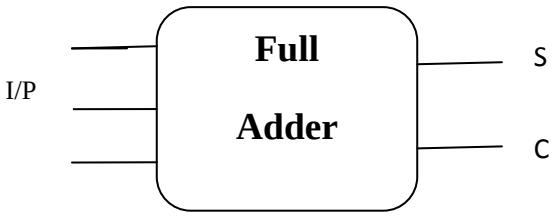

Fig.4 Full Adder

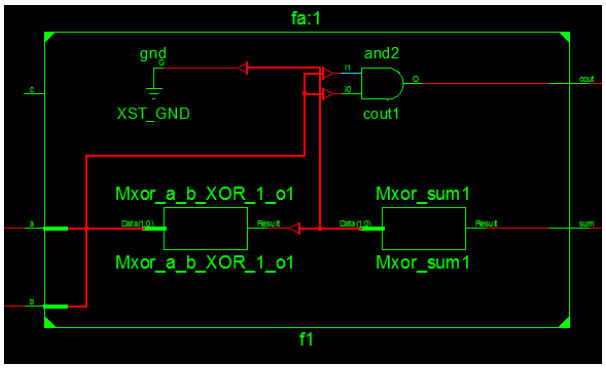

Fig.5 Schematic of Field Array

3.1.3. Compressor

The 3:2 compressor is consists of special circuit and two multiplexer. In this the three input and two output. The 4:2 compressors consist of two special circuits and four multiplexer. In this the five input (one being a carry in) and three output (two carries and the sum). The 5:2 compressors consist of two 3:2 compressor. It is widely used compressor. It has seven inputs of which five are direct inputs and two are carry-in bits from a previous stage. Similarly, there are four outputs of which two are carry-out bits to the next stage and the other two are sum and carry bits. All the 5:2 compressors of different designs abide by the generic equation.

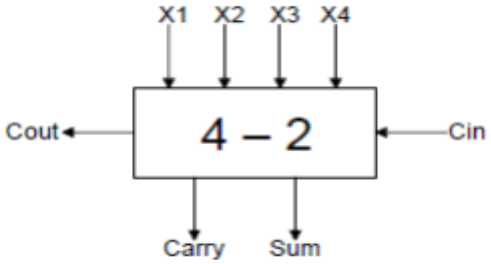

Fig.6 Block diagram of the 4-2 compressor

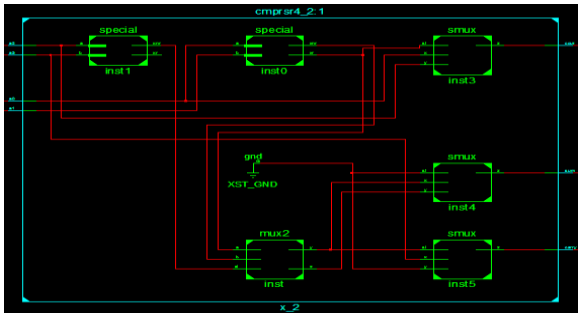

Fig.7 Schematic of 4:2 compressors

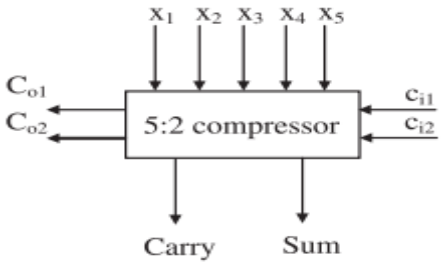

Fig.8 Block diagram of 5:2 compressor

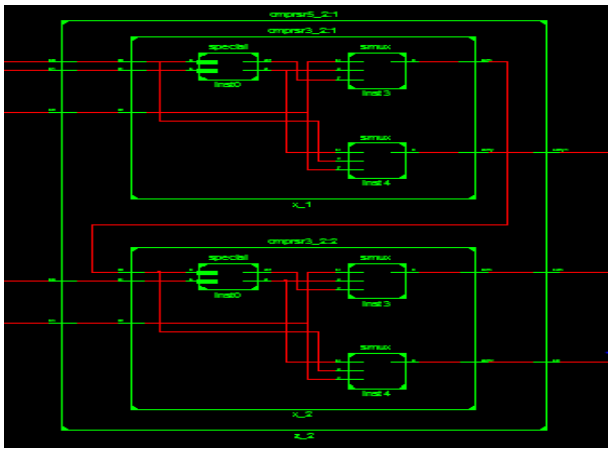

Fig.9 Schematic of 5;2 compressor

4. RESULTS

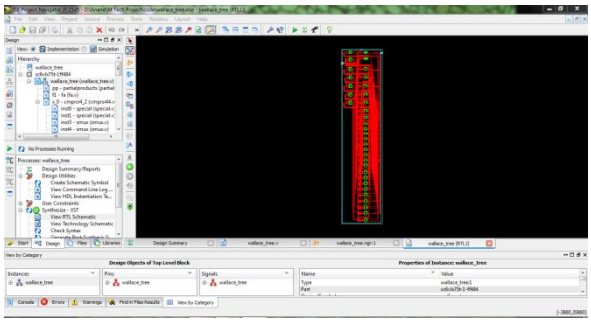

Fig.10 RTL Schematic Wallace tree Multiplier

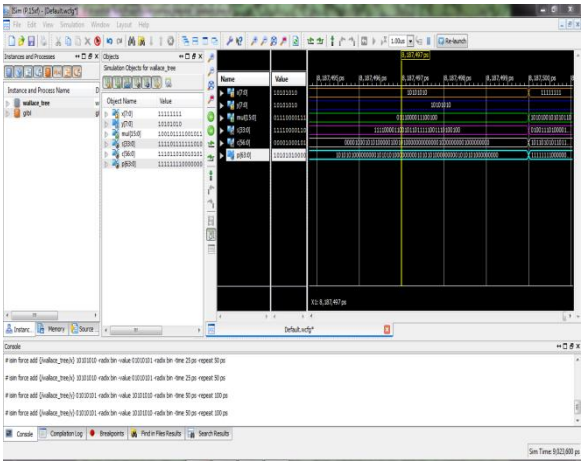

Fig.11 Simulation of Wallace tree

Table 1 Comparative result of proposed reversible signed multiplier circuits

Method	Power Dissipation	Number of bonded IOBs	Number of Slice LUTs
Proposed (8x8)	0.034 w	32	70
[13] (5x5)	0.042 w	46	Not known

Table 1 shows Comparative results of proposed reversible signed multiplier circuit. In this table, we compare the power dissipation of proposed design with existing design in [13].

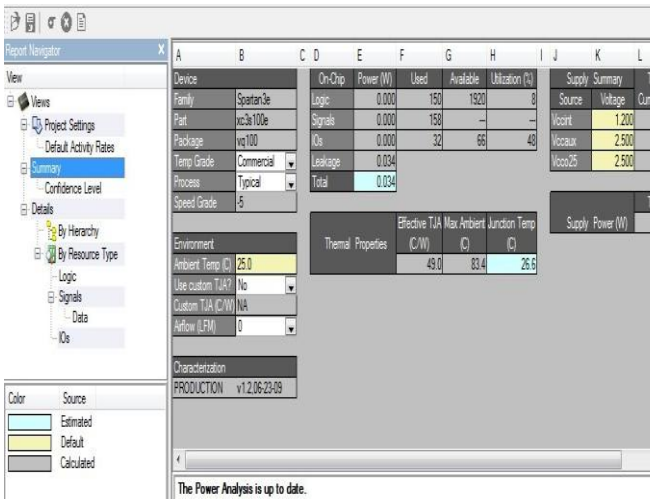

Fig.12 Power dissipation after post extraction simulation for reversible multiplier

5. CONCLUSION

In this paper, we tend to given a unique 8x8 bit reversible multiplier circuit using HNG gates. The planned reversible multiplier circuit is better than the present designs in terms of hardware complexness, variety of gates, garbage outputs and constant inputs. During this paper, planned the planning techniques and methodology to implementation of Wallace reversible signed multiplier circuit in ASIC. Our planned reversible multiplier circuit is applied to the design of difficult systems in nanotechnology.

6. REFERENCES

[1] Hatkar A.P., Hatkar A.A., Narkhede N.P., "ASIC Design of Reversible Multiplier Circuit," International Conference on Electronic Systems, Signal Processing and Computing Technologies, Journal 16, 2014, pp. 47-51.

[2] C. H. Bennett, "Logical reversibility of computation," IBM Journal of Research and Development, Vol.-17, Issue-6, Nov-1973, pp. 525-532

[3] E. F. Fredkin and T. Toffoli, "Conservative logic," International Journal of Theoretical Physics, Vol.-21, No.-3/4, 1982, pp. 219-253.

[4] T. Toffoli, "Reversible computing," in Automata, Languages and Programming, W. De Bakker and J. Van Leeuwen, Eds. Springer, 1980, pp. 632.

[5] A. Peres, "Reversible logic and quantum computers," Phy. Rev. A, 32, 1985, pp. 3266-3275.

[6] M. Haghparast, Somayyeh Jafarali Jassbi, K. Navi and Omid Hashemipour, "Design of a Novel Reversible Multiplier Circuit using HNG Gate in Nanotechnology," World Applied Sciences Journal 3(6), 2008, pp. 974-978.

[7] Neil Weste, Kamran Eshraghin, "Principles of CMOS VLSI Design," Second Edition, 20002.

[8] Vijay K Panchal, Vimal H Nayak, "Analysis of Multiplier Circuit Using Reversible Logic" International Journal for Innovative Research in Science & Technology, Vol.-1, Issue-6, Nov-2014, pp. 279-283.

[9] Md. Belayet Ali, Hosna Ara Rahman and Md. Mizanur Rahman, "Design of a High Performance Reversible Multiplier," IJCSI International Journal of Computer Science Issues, Vol.-8, Issue-6, No.-1, 2011, pp. 134-141.

[10] Mariam Zomorodi Moghadam, Keivan Navi, "Ultra-area-efficient reversible multiplier," Microelectronics Journal 43, 2012, pp. 377-385.

[11] Rigui Zhou, Yang Shi, Huian Wang, Jian Cao, "Transistor realization of reversible "ZS" series gates and reversible array multiplier," Microelectronics Journal 42, 2011, pp. 305-315.

[12] Ehsan Pour Ali Akbar, Majid Haghparast, Keivan Navi, "Novel design of a fast reversible Wallace sign multiplier circuit in nanotechnology," Microelectronics Journal 42, 2011, pp. 973-981.

[13] R. Landauer, "Irreversibilty and heat generation in the computing process," Reprinted from IBM Journal of Research and Development, Vol-5, Issue-3, 1961, pp. 183-191.