Implementing RNS Arithmetic unit through Single Electron Quantum-dot Cellular Automata

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ABSTRACT
Moving toward nanotechnology, many brand new applications are emerging in order to make synergy and mutual benefits from different knowledge areas. In this era, many efforts have been devoted to Quantum-dot cellular automata (QCA) technology as one of the main substitution for conventional Complementary-Metal-Oxide-Semiconductor (CMOS).

On the other hand, rather than focusing on minimizing devices and area, other groups were working on increasing functionality speed. One of the main fields that many researchers investigated on was Residue number system (RNS).

Working on Cell designs for improving QCA cell functionality and circuit implementing, a novel method named SE QCA has been proposed which was reducing critical path and power consumption in advance. [1] Because of applying these cells on inverter and majority gates as basic components of QCA logics, a well-optimized design with minimum cell numbers are proposed. Accordingly, based on the fundamental and significant role of full adder modules in digital systems, a novel efficient full adder is presented as well.

Hence, in this article, mentioned above concept is used and it is tried to optimize the implementation of RNS arithmetic unit through QCA. The simplified arithmetic unit of RNS, is designed in QCADesigner 2.0, and is optimized through single quantum-dot cellular as a result.

General Terms
Computing, arithmetic, nanotechnology.

Keywords
Quantum-dot Cellular Automata, Residue Number System, Single Electron QCA, Full Adder Cell, Arithmetic unit.

1. INTRODUCTION
Challenging with high leakage current, power consumption and cost of lithography, CMOS technology faced with several nanotechnologies to be replaced by such as Carbon Nano-Tube Field Effect Transistors (CNFETs), Graphene Nano-Ribbons transistors (GNRs), Single Electron Transistors (SETs) and Quantum-dot cellular automata (QCA). Quantum-dot cellular automata is originally proposed by Lent et al. at 1993[2].

Metal Island, Magnetic, semiconductor, and molecular methods are proposed for fabrication of a QCA cell, which is composed of four dots, placed at the corners of a square shape as illustrated in Fig. 1(a). Traditionally, in all of these methods, two excess electrons have been injected into the cell. According to the columbic interaction, these two electrons have been forced to have two possible configurations as shown in Fig. 1(b); consequently, QCA binary states are expressed in situations of these two electrons rather than voltage levels, as cell's polarization (P=+1, P=-1) and encoded to logic states of "1" and "0", respectively. The electrons can be transmitted between dots via tunneling junctions by inducing suitable voltage from outside. A QCA wire can be constructed by placing several cells side-by-side [3].
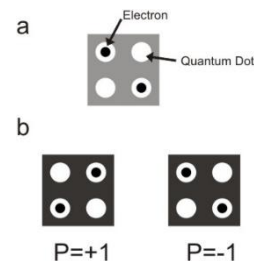

Fig. 1 (a) QCA basic cell with two electron. (b)Two possible configurations of electrons in QCA cell

The fundamental elements including wire, Invertor, and majority gates are used for designing QCA circuits (Fig. 2). As it is illustrated in Fig. 2(a), various types of inverter with different structures are presented [7]. It is to be noted that by fixing one of the input's polarizations to -1 or +1, Three Input AND gate or Three Input OR gate will be achieved at the device cell. Following equations show this fact.

$$M\ (A,\ B,\ C)\ =\ AB\ +\ AC\ +\ BC \quad (1)$$

$$M\ (A,\ B,\ 0)\ =\ AB\ +\ (A)(0)\ +\ (B)(0)\ =\ AB \quad (2)$$

$$M\ (A,\ B,\ 1)\ =\ AB\ +\ (A)(1)\ +\ (B)(1)\ =\ A\ +\ B \quad (3)$$

The main concept in QCA functionality is realizing its clocking phases. There are four clocking phases (Switch, Hold, Relax, and Release) in every QCA circuit and a computation process runs by sequentially performing of these four phases. During the switch phase, electrons can be excited for transmitting between dots due to the neighbor polarizations. In the hold phase, cells keep their polarization and only can effect on the other cells. During relax and release phases, cells lose their polarizations and remain un-polarized until next excitation [6]. The QCA clocking is achieved by managing the potential barriers between adjacent quantum dots. Controlling the potential barrier by raising or lowering

allows full control of localization and polarization for the mobile electrons as follows: raising potential force elements to localize and hence definite polarization occur while the lowering potential allows delocalizing electrons and providing no definite cell polarization.
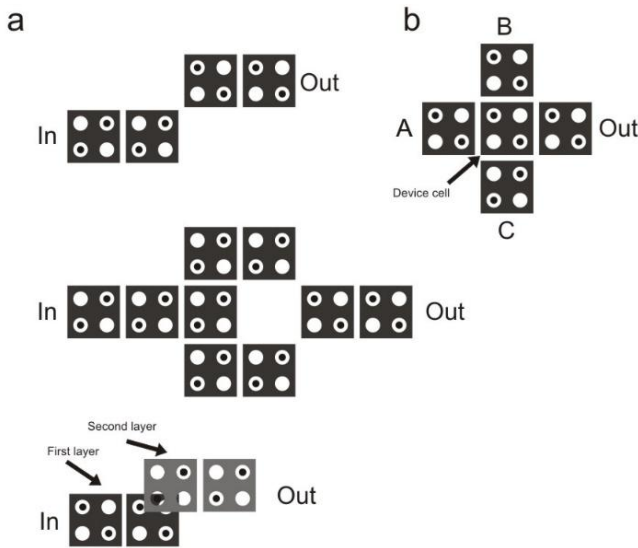
Fig. 2 Basic QCA structures (a) Various types of inverters. (b) Three-input majority gate.

Several efforts have been made to introduce various types of a QCA cell in order to reach more appropriate operation with less area, and more speed. Robustness is a challenge of these models. Most of these cells have been used for executing Multi-value logic (MVL) in QCA. MVL offers a specific perception in the field of calculation and is an intermediate state among binary and fuzzy systems that can take the benefits of having multiple states [4-6]. The latest cell design was introduced by [1] which is called Single Electron QCA cell. It considers current clocking method, and similar standard cell dimension, which leads to use simultaneously in a hybrid design.

After Introducing the fundamental concepts of QCA technology, the rest of the article is combined of a summary on Residue Numbers, and introducing the functionality of SE QCA. Afterward, the methods of how to implement RNS arithmetic unit through SE QCA. In the last section comparison between previous works and the proposed solution is provided which shows significant improvements in different indicators.

All the proposed designs in this paper have been simulated using coherence simulation engine with clock high = $9.8e-22J$ and clock low = $3.8e-23$ J [4].

2. RESIDUE NUMBER SYSTEMS (RNS)

The most significant characteristics of Residue Number systems are high-speed and parallel computation capability, carry free nature, secure communication based on fault tolerant architecture and ease of detection and correction of errors.

RNS is proposed with a moduli set of positive integers, {m1, m2, m3, …, mL}. In case of using pairwise coprime moduli, maximum dynamic range [α, α +M) will be achieved in which α is an integer and $M = \prod_{i=1}^{L} m_i$. Hence, $x_i = X \bmod m_i, i = 1,2,…,L$,which indicates that X in binary system ($\alpha \leq \times < \alpha + M$) will be shown in RNS system with a set of remainders $(x_1, x_2, x_3 … x_L)$.

Lower power consumption and more speed up, are the main reasons of using RNS system. In comparison with Binary system, there would be no carry propagation issue any more. However, most of popular digital systems operate in Binary system. In contrast, RNS is using in certain processors, for instance, in DSP, Image processing, digital filters, and encryptions.[8]

On account of the fact that RNS functionality is based on simple add, subtract and multiply functions, here as a sample, add function between 2 positive integers A and B in RNS system is formulated:

$$(A + B)_{10} \Leftrightarrow ||A|_m + |B|_m|_m$$

Other functions, have the same formulas.

Considering decomposition of a RNS computational system, 3 sections will be reached, as shown in Figure 3: Binary to Residue Converter (Forward Converter), Computational unit (Arithmetic Unit), and Residue to Binary Converter (Reverse Converter).
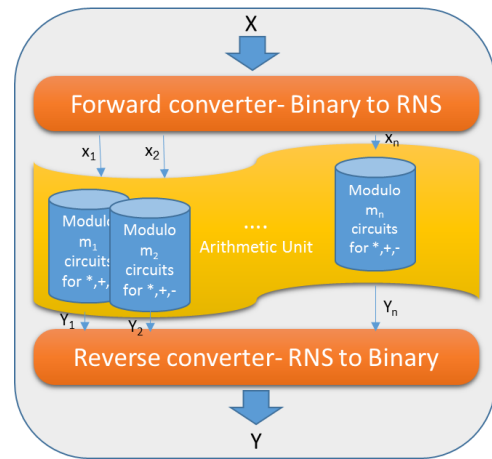
Fig. 3 general block diagram of RNS system

In order to convert an integer X (k bits) into a reside Number (x1, …, xn) where $x = \sum_{j=0}^{n} x_j 2^j$, in which $\forall x_j \in \{0,1\}$, and for moduli {p1,…pn}, the below formula will be achieved:

$$|x|_{p_i} = \left| \left| \sum_{j=0}^{n} x_j |2^j|_{p_i} \right| \right|_{p_i}$$

For reverse converter, famous algorithms have been proposed such as Chinese Remainder Theorem, Efficient MRC-Based Residue to Binary Converters, etc. [9]

However, based on the high frequency operation of Arithmetic unit, it became the most important part of RNS system, and in this article our concentration is Arithmetic Unit.

2.1 Arithmetic Unit in RNS system

In order to build up an adder block in Residue system, considering Kbits A and B, as shown in Figure 4, the below constraints are existed:

- If the result of sum becomes less than moduli, the result is the answer

- If the result of sum becomes equal or more than moduli:

- The moduli should be subtracted from the result
- Or, the result should be added with its complementary, and the result will be the add residue in the moduli.

The formula, indicates the addition function in RNS system between K bits A and B is shown below:

$$|A+B|_p = \begin{cases} A+B-P+2^k-2^k & , \ A+B+2^k-P \geq 2^k \\ A+B & , \ otherwise \end{cases}$$

$$= \begin{cases} |A+B-P+2^k|_{2^k} & , \ A+B+2^k-P \geq 2^k \\ A+B & , \ otherwise \end{cases}$$

General block diagram of the above-mentioned function is shown in figure 4.
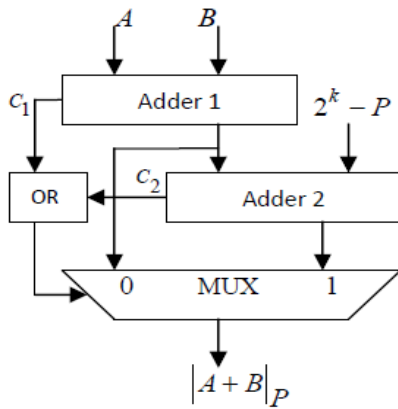
Fig4 .General diagram of a moduli adder

Another block diagram also shown in figure 5, which indicates adder/subtraction in RNS system for two n bits A and B integer.
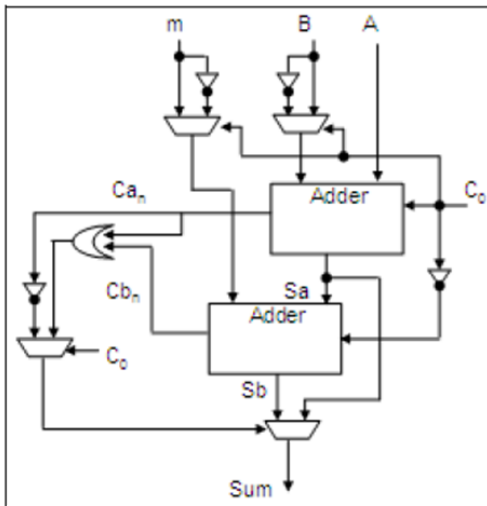

Fig. 5 An Adder/Subtractor block diagram in RNS[9]

The result of the above diagram, for addition and subtraction are shown below orderly:

$$|A+B|_m = \begin{cases} A+B-m & \text{if } A+B \geq m \\ A+B & \text{otherwise} \end{cases}$$

$$|A-B|_m = \begin{cases} A-B+m & \text{if } A-B < 0 \\ A-B & \text{if A - B} \geq 0 \end{cases}$$

Considering X,Y, and S in RNS system with moduli n:

$$X = (x_1, x_2, \cdots, x_n)$$
$$Y = (y_1, y_2, \cdots, y_n)$$
$$S = (s_1, s_2, \cdots, s_n)$$

In the case $0 \leq s_i < m_i$, operation $\otimes$ in formula below can be used for addition, subtraction, and multiplication:

$$S = X \otimes Y \rightarrow \quad s_i = |x_i \otimes y_i|_{m_i}$$

3. SINGLE ELECTRON QCA

Proposed architecture for Single electron QCA cell (SE QCA) is shown in Figure 6, containing four quantum dots and a single electron. This electron can occupy each of the dots according to the electrostatic repulsions of its neighbor cells. This provides a four state QCA cell, which is entitled by A, B, C and D letter in Figure 6. Regarding the physical proofs, the length of 18 nm for the square's sides and the value of 2 nm for cell to cell distance are considered. Single electron QCA cell (SE cell) is developed to apply as a transient cell and use the same clocking mechanisms that regular double electron cells use which leads to have an easy combinational design of both. The potential energy [10] between two excess electrons can be expressed as following equations:

$$U = K \frac{Q_i Q_j}{r}$$

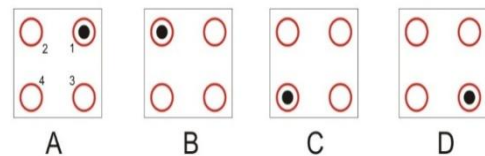$$U_T = \sum_{s=1}^{n} U_s$$

Fig. 6 The proposed cell architecture with four dots and only one electron. Due to the neighbor's polarization, the single electron can occupy each one of the 1, 2, 3 or 4 quantum dots. [1]

It is clear that in order to achieve more stability in a QCA cell; electrons must be arranged in more distance from each other for reaching the minimum state of potential energy. It is supposed that the electrons located at the square's corners in calculations. This means that the near-neighbor distance between two electrons is taken to be 18 nm, this assumption will not affect the results. In the above equation, U represents the potential energy between two electric charges. Here Qi and Qj are the electric charges, K is fixed colon, and r represents the distance between two charges. UT indicates the summation of potential energies for a single electron.

Physical proofs of how wire embedded inverter, and minatory voter gate acts in QCA system is completely discussed in [1].

From the arithmetic point of view, the addition is a basic operation for subtraction, multiplication and division

operations that are widely used in digital systems. Therefore, to implement a novel and efficient QCA full adder, by using minatory voter gates and inverters, an optimized Full adder has been proposed.

As it is illustrated in Figure7, applying the three-input minority gate new one-bit full adder cell schematic with only two gates.
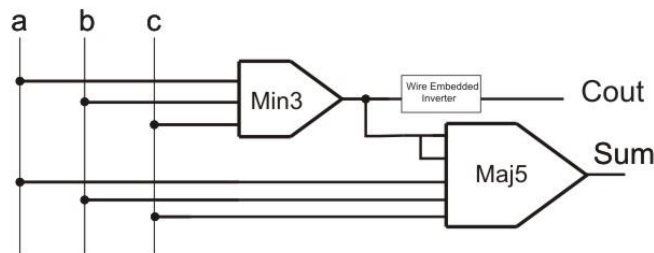

Fig. 7 one-bit full adder cell schematic with two gates

# 4. USING SE QCA FOR IMPLEMENTING RNS ARITHMETIC UNIT

Based on the fact that Majority voter gate is the fundamental element in QCA technology, there should be a method to convert the circuits into majority based design. Table 1 shows different majority based design of functions such as And, Or, Nand, Xor, and Xnor in QCA Coplanar layout. In this regards, comparison between ordinary QCA and SE QCA is presented which shows a better improvement in less occupied area and less number of cells used.

For instance, Xor and Xnor show 30 percent improvement in area and number of cell used.

Table 1 Implementing computational operators through majority based QCA design and SE QCA

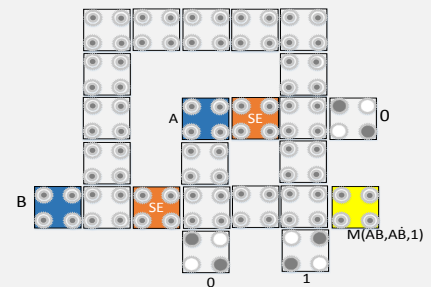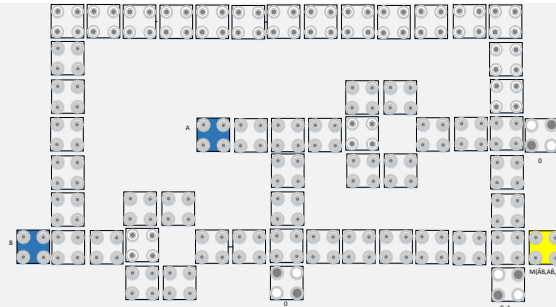| *Function and its formula*	*Majority based coplanar design in QCA*	*Coplanar design in SE QCA*
$F(and) = A.B$		
$F(or) = A + B$		
$\overline{F(nand)} = \overline{A.B} = \bar{A} + \bar{B}$		

$F(nor) = \overline{A+B} = \bar{A}.\bar{B}$
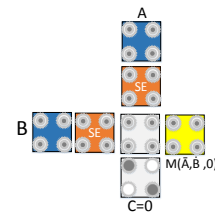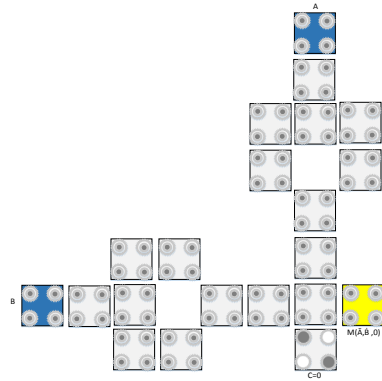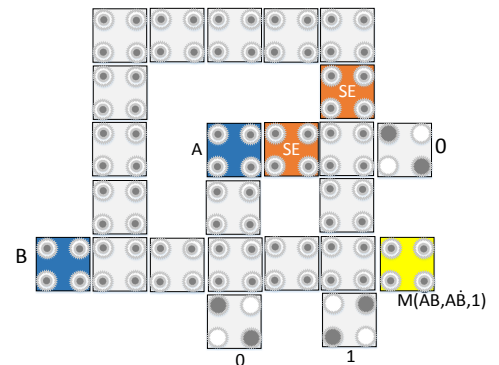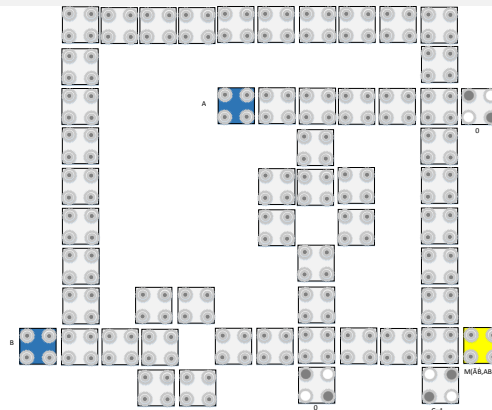

$F(xor) = A \oplus B$

$= A\bar{B} + \bar{A}B$

$F(xnor) = A \odot B$

$= \bar{A}\bar{B} + AB$

Area improvement (55 cells decrease to 24), delay improvement (3 clocks)

In order to implement RNS arithmetic unit in QCA, Cellular pipeline array method is considered, which includes interconnection of sub-logical circuits called cells or processing elements (PE). Different designs of cellular pipeline array are proposed [11]. The reference model proposed I [12] in capable for all arithmetic functions which has separate functional and control units.

In summary, an arithmetic cell used in the cellular pipeline array which is considering in our model, is shown in figure 8. Inputs A,B, and C are operational inputs; and F, and X are controlling signals. This block can handle the bellowed operations:

$S = [A \oplus (B \oplus X) \oplus C_1]F_i + A\bar{F_i}$

$C_0 = (B \oplus X)(A + C_1) + AC_1$
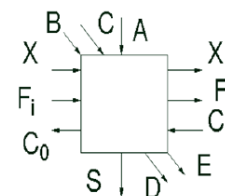
$D = C(B + F_i)$

$E = (B + C)(B + F_i)$

Fig. 8 An arithmetic cell diagram [12]

There is a brief table (table.2) shows how operations are valuated based on different values of controlling signals. [12]

**Table2 operation values based on value of controlling signals [12]**

Operator types	Signal values	Operations
+	X=0, Fi=1	$S = A \oplus B \oplus C_1$
-	X=1, Fi=1	$S = A \oplus \bar{B} \oplus C_1$
$\times$	X=0, A=0, B=C	A multiply B. right shift add method
$\div$	X=1, B=C, P=0	B divided by A. right shift method
( )^2	X=0, A=0	B is a 2nd complement of digit 10. C=10, Operand: A
$\sqrt{}$	X=1, P=0	B is a 2nd complement of digit 10. C=10. Operand: B
$\sqrt{}$	X=1, P=0	B is a 2nd complement of digit 10. C=10. Operand: B

Based on the proposed design by Dajani [9], customized design which is implementable in QCA system, and also its corrected layout in QCADesigner are respectively shown in figure 9,10.
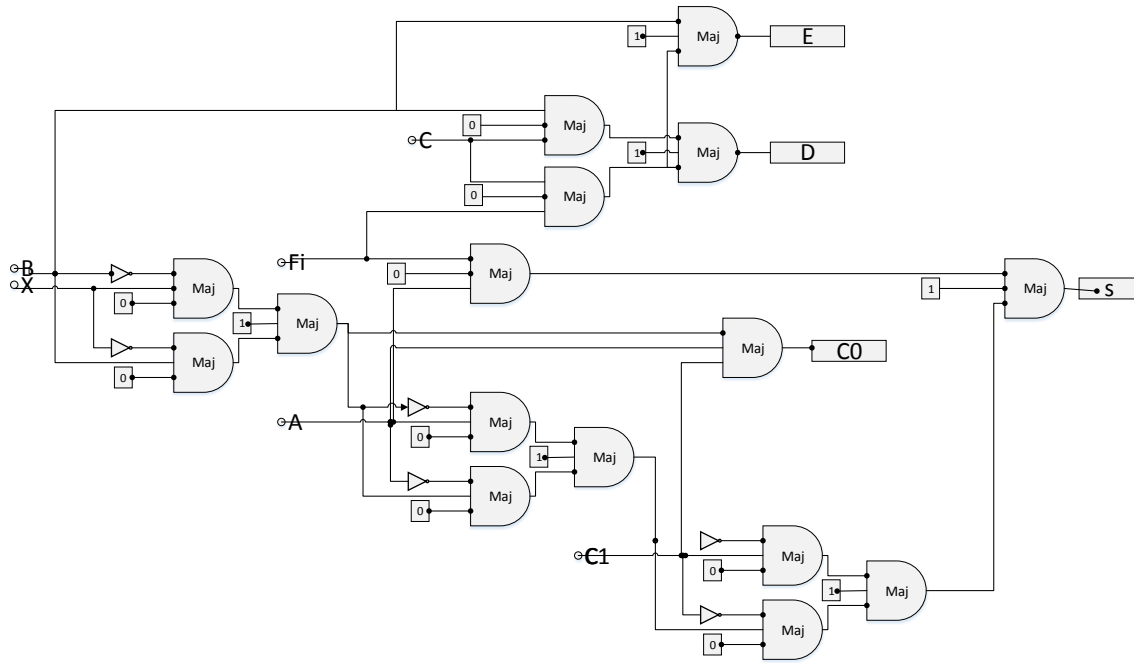

a) Arithmetic Cell
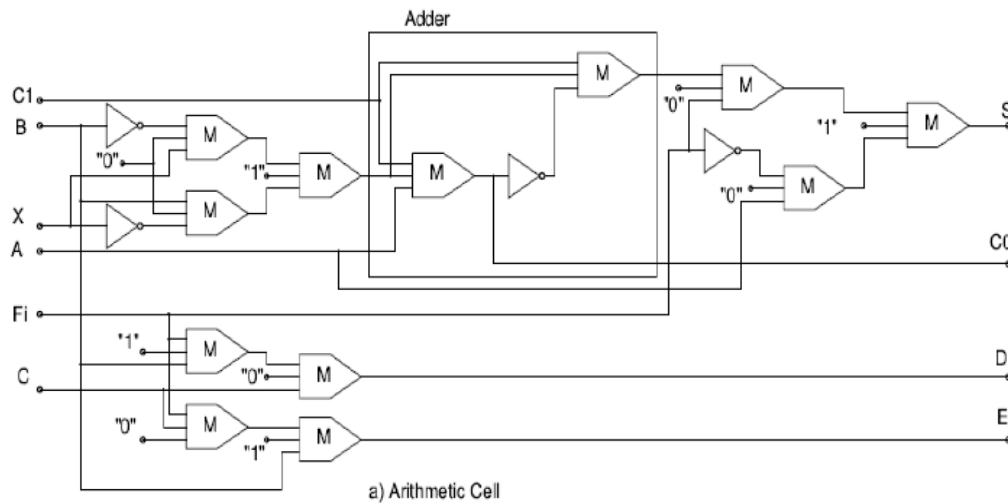
Fig. 9 Implementable RNS arithmetic unit in QCA [9]
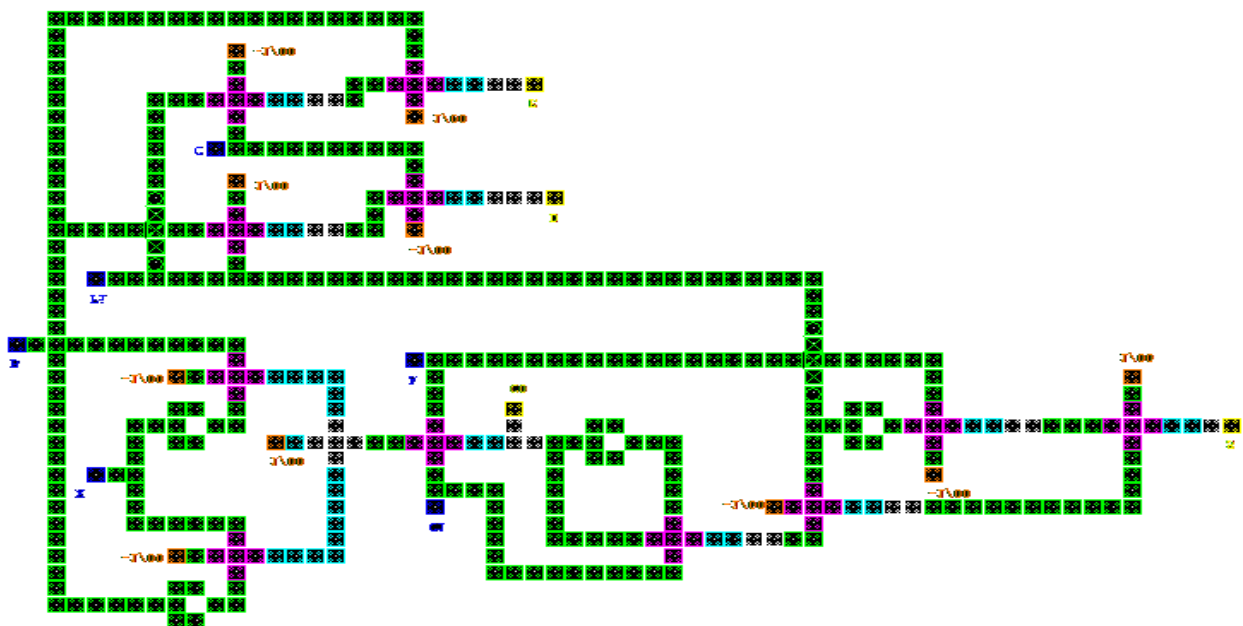
**Fig. 10 corrected QCA layout for Dajani proposed circuit in fig.8**

The proposed design which is correctly working based on

pipeline architecture is shown in figure 11.

Fig. 11 proposed circuit design for RNS arithmetic unit, implementable in QCA

Rather than proposed optimization circuit design in figure 11, the self-optimized SE QCA cell makes our design to have the

best performance in comparison with previous works which its layout is shown in figure 12.
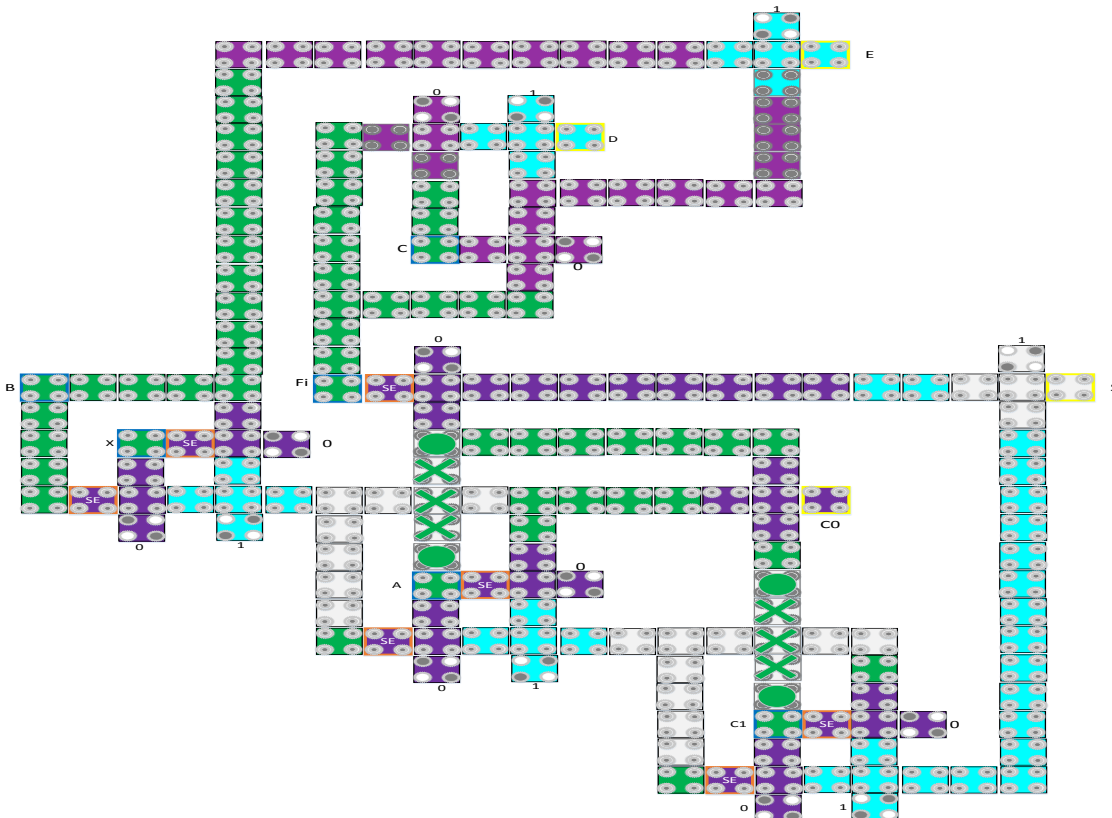
Fig. 12 Proposed SE QCA design for RNS arithmetic unit

5. CONCLUSION

As a conclusion, this work presents a new implementation of RNS Arithmetic Unit circuit through Single Electron QCA technology which has a better performance in comparison to previous works. Levering SE QCA cells in QCA

implementations will lead to have more optimized designs in terms of power, area, and cell counts. Applying SE cells in QCA digital systems will result in circuit improvements in terms of cells count, propagation delay and occupation area.

The comparison between three available designs in illustrated in table 3. In this comparison, occupied area of each SE QCA cell is supposed equal to a standard QCA cell. Furthermore, previous works are redesigned and the figures achieved are different from the references proposed by their owners.

Table3 performance comparison between 3 available designs for RNS arithmetic units

Parameters	Proposed SE QCA	Dajani design	Agrawal design
# of Cells	393	439	**1004**
# of I/Os	10	10	**14**
# of Majority gates	11	15	**28**
# of Not gates	0	5	**10**
Covered area (um2)	0.78	0.94	**1.46**
Max delay time(Ps)		0.785	**0.911**
Operating Voltage	5	5	**5**

According to the contribution proposed in this paper, new applied technics can be used between QCA and RNS in order to reduce the area and speed up the arithmetic calculation which is the basic of computation. Rather than Arithmetic unit which is focused in this article, new researches can be investigated to complete the RNS system implementation as well.

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