# FPGA Implementation of Digital Modulation Techniques BPSK and QPSK using HDL Verilog

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## ABSTRACT
In the wireless communication system, to transfer the data without loss and to reduce size of antenna, modulation is the most important technique. Phase-shift keying (PSK) is a modulation technique in which the phase of a transmitted signal varies to convey information. Binary Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying (QPSK) are implemented in Field Programmable Gate Array (FPGA). The proposed designs are aimed for study purposes. These digital modulators are designed using Verilog Hardware Description Language (HDL). Cadence's NC-Sim simulation software is used to check the functionality of designs. Xilinx's integrated software Environment (ISE) used for FPGA design implementation.

## Keywords
BPSK, QPSK, FPGA, DDS (Direct Digital Synthesizer), ROM (Read Only Memory), LUT (Look Up Table)

## 1. INTRODUCTION
In the modern wireless technology operating speed, area and power consumption of an electronic circuit are very important parameters. These parameters play an important role to reduce the area and cost of an electronic circuit and to improve the performance. FPGAs are programmable semiconductor devices consist of a matrix of Configurable Logic Blocks (CLBs) connected through programmable interconnects. It has random-access memories (SRAMs), high-speed transceivers, high-speed input/output (I/O) elements, network interfaces, and even hard-embedded processors. FPGAs can be programmed to the desired application or functionality requirements. FPGAs allow designers to change their designs very late in the design cycle, even after the end of production and deployed in the field. The communication system based on FPGA is easy to implement and simple to upgrade. A literature survey shows that FPGAs are widely used in different applications [1], [2]. BPSK, QPSK are type of digital modulation technique [3] used to transfer the baseband data wirelessly in much efficient way compare to other modulation techniques. Generally a conventional BPSK/QPSK modulator with Direct Digital Synthesizer (DDS) and arithmetic multiplier consumes high power and low throughput with complexity in hardware implementation. Hence to generate high throughput BPSK/QPSK modulator, the first proposal uses DDS Intellectual property (IP) provided by Xilinx. The second proposed method produces the BPSK/QPSK signal which is based on stored BPSK/QPSK phase data in ROM. This method eliminates completely the DDS and multiplier blocks of the modulator. The modulator design has been made generic so that it can be used as either BPSK or QPSK by use of single operational switch. The paper is organized as follows. In Section 2, the theory of Digital Modulations BPSK/QPSK modulation techniques are briefly explained. In Section 3, the proposed methodology with building blocks of the all-digital design to be implemented in an FPGA are given, with details. The verification of the implemented digital modulators through simulations and results acquired from the implementation into the Xilinx's FPGA are emphasized and evaluated in Section 4 and 5. Finally, in Section 6, conclusions are drawn.

## 2. DIGITAL MODULATION
The advantages of digital modulation [4] as compared to the analogue counterpart as less complex, more secure, more efficient in long-distance transmission and noise detection/correction. In digital modulation techniques, an analogue carrier signal is modulated by a binary code.

### 2.1 BPSK Modulation
In a BPSK modulation process, the phase of the sinusoidal carrier signal changes according to the message level ("0" or "1") with amplitude and frequency constant. BPSK is one of the simplest PSK modulation techniques. It uses two phases (0 and 180 degrees). Figure 1 shows BPSK modulation. A BPSK signal can be expressed is described by (1). Where binary message as *m (t)* = 0 or 1, Bit duration as *T*, Amplitude as *A*, and Carrier Frequency $f_c$.

$$S(t) = A\,Sin\,[2\pi f_c t + m(t)\pi], 0 \le t \le T \quad (1)$$

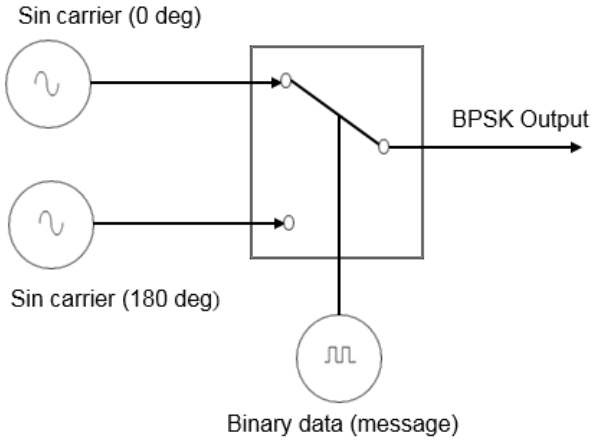


**Figure 1: BPSK Modulation**

### 2.2 QPSK Modulation
The implementation of QPSK [5], [6] is more general than that of BPSK. This includes the two bandwidth conserving modulation schemes for the transmission of binary data. The Quadrature-carrier multiplexing system, which produces a modulated wave is described by (2).

$$S(t) = S_I\,Cos\,[2\pi f_c t] - S_Q\,Sin\,[2\pi f_c t] \quad (2)$$

Where In phase component as $S_I(t)$, Quadrature phase component as $S_Q(t)$, and Carrier Frequency $f_c$. In QPSK, the phase of the carrier takes on one of four equally spaced values as 225º, 315º, 135 º, 45 º. For this set of values, we may define the transmitted signal described by (3).

$$S_i(t) = \begin{cases} \sqrt{\frac{2E}{T}}\ Cos\left[2\pi f_c t + \frac{(2i-1)\pi}{4}\right], & 0 \le t \le T \\ 0\ , \ Elsewhere \end{cases} \quad (3)$$

Where $i$ an integer value as 1, 2, 3, 4, Transmitted signal energy as $E$, and the symbol duration as $T$. Each possible value of the phase corresponds to a unique pair of bit stream as 00, 01, 10, 11, and then equivalent form of the modulated signal can be rewritten for (3) as described by (4).

$$S_i(t) = \begin{cases} \sqrt{\frac{2E}{T}}\ Cos\left[\frac{(2i-1)\pi}{4}\right] Cos(2\pi f_c t) - \\ \sqrt{\frac{2E}{T}}\ Sin\left[\frac{(2i-1)\pi}{4}\right] Sin(2\pi f_c t)\ , \ 0 \le t \le T \\ 0\ , \ Elsewhere \end{cases} \quad (4)$$

There are only two orthonormal basis functions I-Phase and Q-Phase. Expansion is described by (5) and (6).

$$S_I = \sqrt{\frac{2E}{T}} Cos\left[2\pi f_c t\right], 0 \le t \le T \quad (5)$$

$$S_Q = \sqrt{\frac{2E}{T}} Sin\left[2\pi f_c t\right], 0 \le t \le T \quad (6)$$

The digital QPSK modulator [7] is as shown in Figure 2. The input binary data sequence is divided into two other sequences, i.e. odd and even numbered bits of the input sequence. These two sequences are in unipolar and changed into bipolar by using Non Return to Zero (NRZ) encoding technique. The coded data gets mixed with carrier which is generated from DDS. The DDS produces the sine and cosine as separate carrier signal of same frequency. After multiplying the carrier signal with bipolar data, the obtained odd data is known as I-phase and the even data as Q-phase. These two phases gets added together to produce a single QPSK modulated signal as described by equation (3). QPSK phase with different input is as shown in Table 1.

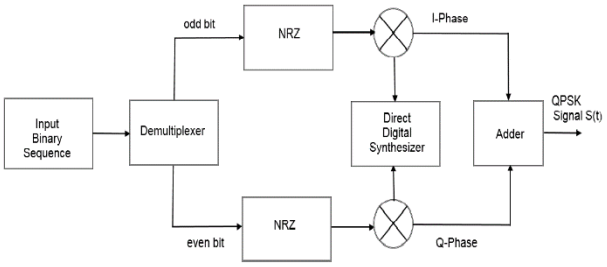


**Figure 2 QPSK Modulation**

**Table 1: QPSK Phase Relation**

| Input | QPSK Phase |
|---|---|
| 00 | 225º |
| 01 | 315º |
| 10 | 135 º |
| 11 | 45 º |

# 3. PROPOSED METHODOLOGY

Two new methods are proposed in BPSK/QPSK [8], [9] modulators. First method uses DDS as IP provided by Xilinx [10], [11]. Second method uses ROM as main data storage to produce same BPSK/QPSK signal.

## 3.1 Proposed QPSK Modulator Modulation Method 1

DDS is used to generate a sinusoidal carrier signal, which is implemented by using different parts: a phase generator (accumulator) and a phase-to-waveform converter (Look up table) as shown in Figure 3.

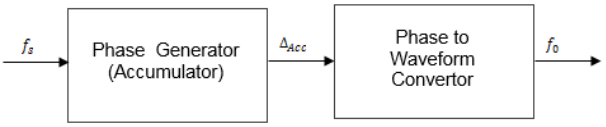


**Figure 3 : Direct Digital Synthesizer**

The accumulator is of size $M$ bits, the period of the output signal is $2\pi$, and the maximum phase is $2^M$. Phase increment of the accumulator output $\Delta_{Acc}$. During each sampling period $T_s$ (sampling frequency $f_s$), the phase is incremented by $\Delta_{Acc}$ to reach its maximum phase value of $2^M$. Second part of the direct digital synthesizer as a phase-to-waveform converter, based on a lookup table (LUT) which stores samples of a sinusoid. The output frequency ($f_0$) of the DDS waveform is a function of the system clock frequency, the number of bits in the phase accumulator ($M$) and the phase increment as described by (7).

$$f_0 = f(f_s, M, \Delta_{Acc}) \quad (7)$$

Output frequency in Hertz is described by (8).

$$f_0 = f_s\ \frac{\Delta_{Acc}}{2^M} \quad (8)$$

The frequency resolution of the synthesizer ($\Delta$f) is a function of the sampling frequency and the number of bits employed in the phase accumulator. The frequency resolution is described by (9).

$$\Delta f = \frac{f_s}{2^M} \quad (9)$$

The phase increment ($\Delta Acc$) defines the synthesizer output frequency and is described by (10).

$$\Delta_{Acc} = \frac{f_0\ 2^M}{f_s} \quad (10)$$

## 3.2 Proposed QPSK Modulator Modulation Method 2

For the second QPSK modulator architecture the above proposed QPSK modulator 1 architecture will be constructed just to collect four different combinational input data for different phases of QPSK. Once the data is collected, the first proposed QPSK modulator architecture will not be used. In this method, data for all four phases of QPSK modulated signal is collected and stored in four different ROM blocks. Each ROM will store the data for one QPSK phase. Free running counter is used to output data from the ROM Since all the four possible phases for a QPSK is stored in four different ROMs, the digital QPSK modulator is no longer required to produce a QPSK phase from I and Q phase as in the first

method of QPSK modulator. The block diagram of proposed QPSK modulator method 2 is shown as in Figure 4. For the simulation purposes, a serial input sequence will be considered as input to the 1:2 de-multiplexer which will separate the input sequence into odd and even bits. These odd and even bits will be the select line input for the 4:1 multiplexer which will select one of the ROM for different combination odd and even bits as 00 for ROM1, 01 for ROM2, 10 for ROM3 and 11 for ROM4.

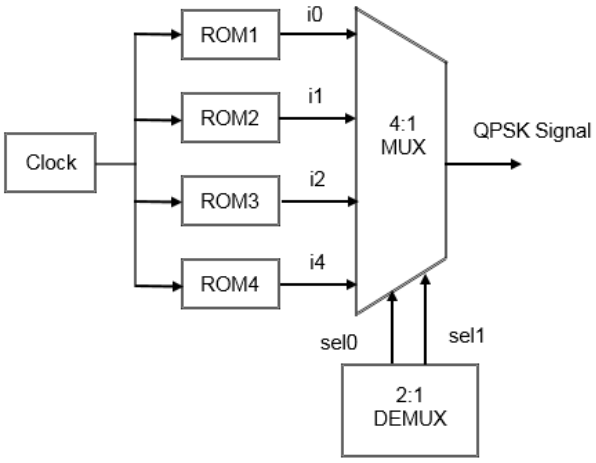


**Figure 4: Block diagram of proposed QPSK modulator**

also analog signal to plot the waveforms. Each of the design Verilog HDL code is synthesized by using Xilinx ISE13.2. The synthesizable code is translated into RTL (Register Transfer level) schematic diagrams. Figure5 Shows the Top level RTL schematic diagram. Figure 6 and 7 shows the timing diagram for proposed QPSK modulator method1 for BPSK and QPSK. Figure 8 and 9 shows the timing diagram for proposed QPSK modulator method2 for BPSK and QPSK. Figure 10 and Figure11 shows RTL schematic diagram for proposed QPSK modulator method 1 and 2.

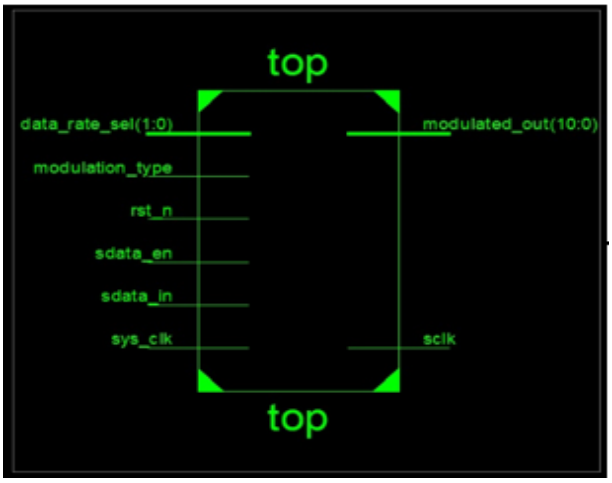


**Figure 5: Top level RTL Schematic diagram**

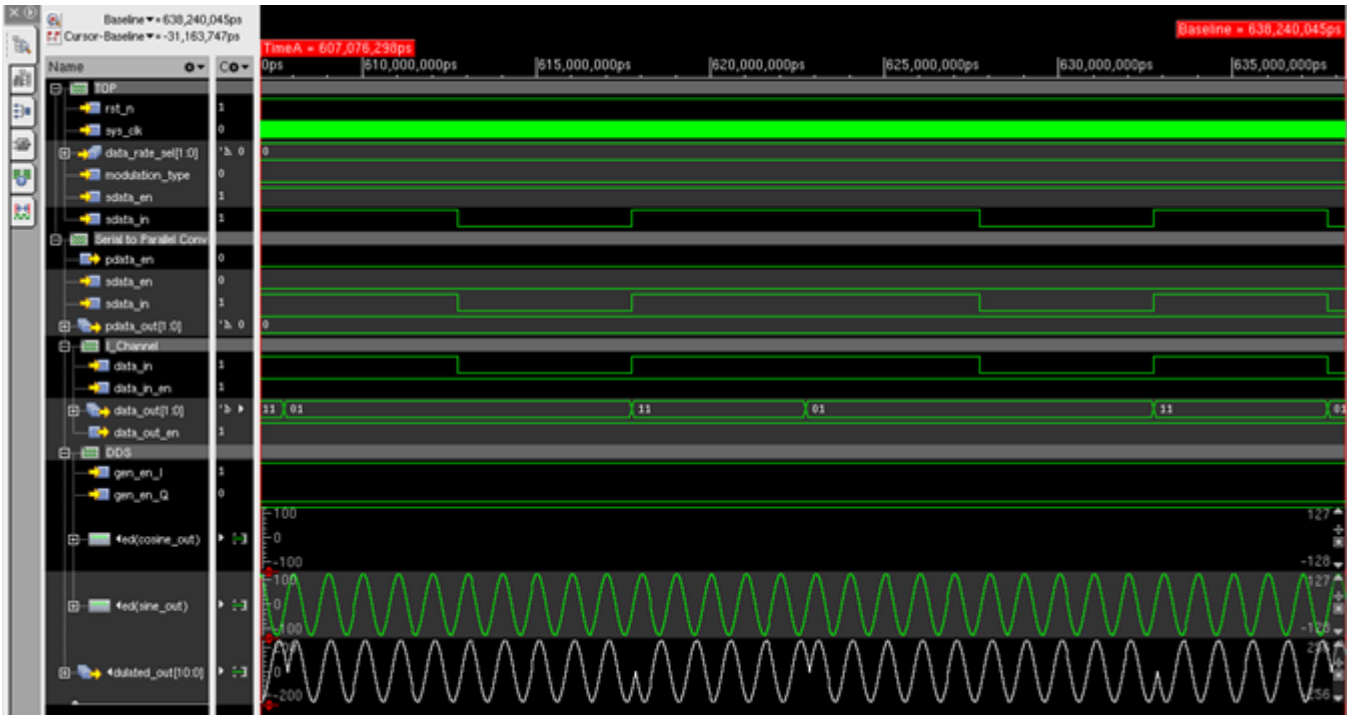


**Figure 6: Simulation result of BPSK modulation method 1**

## 4. SIMULATION

Proposed design and two method of conventional QPSK modulator is modeled with Verilog HDL [12], [13] and simulated using Cadence NC-Sim 15.10-s011. The crucial aspect for simulating the conventional QPSK modulator is to compare with the proposed QPSK modulator in term of high throughput i.e., timing in Xilinx's xc3s50-5pq208 FPGA. The simulator is used to produce the binary or decimal data and

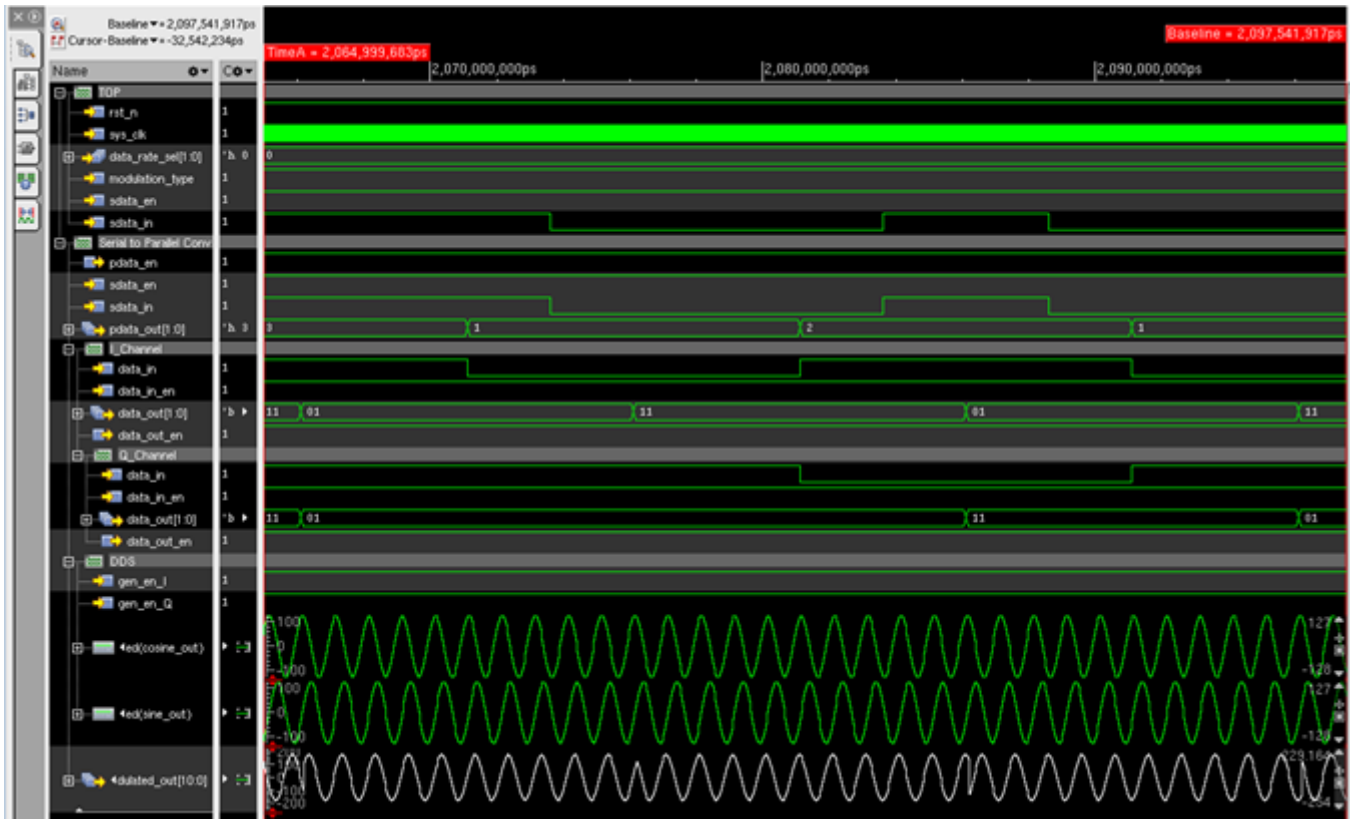


**Figure 7: Simulation result of QPSK modulation method 1**

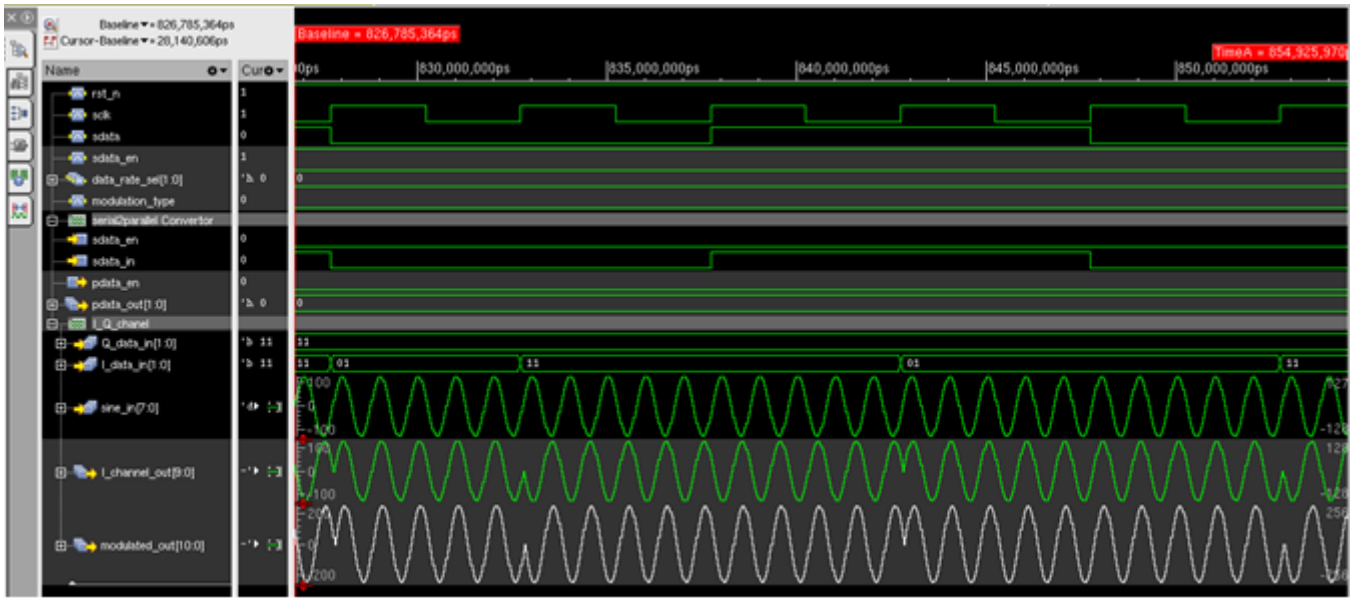


**Figure 8: Simulation result of BPSK modulation method 2**

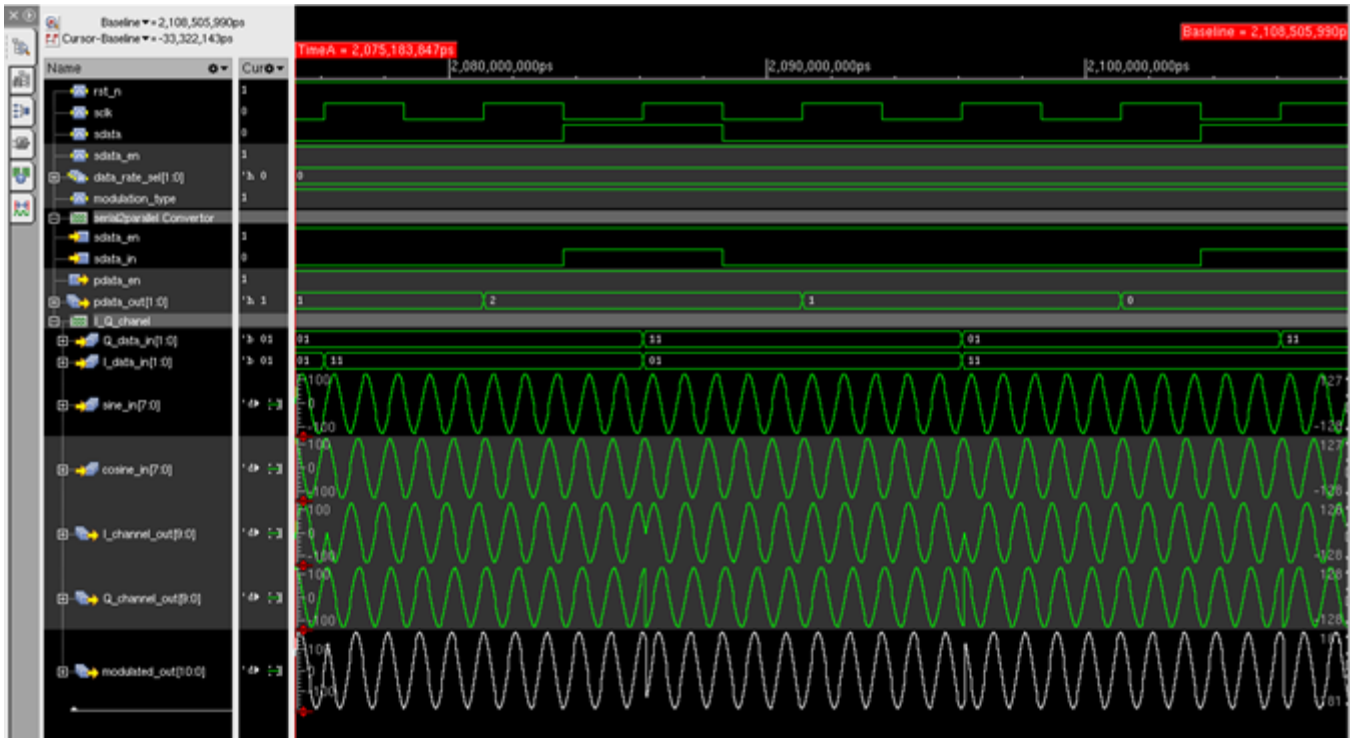


**Figure 9: Simulation result of QPSK modulation method 2**

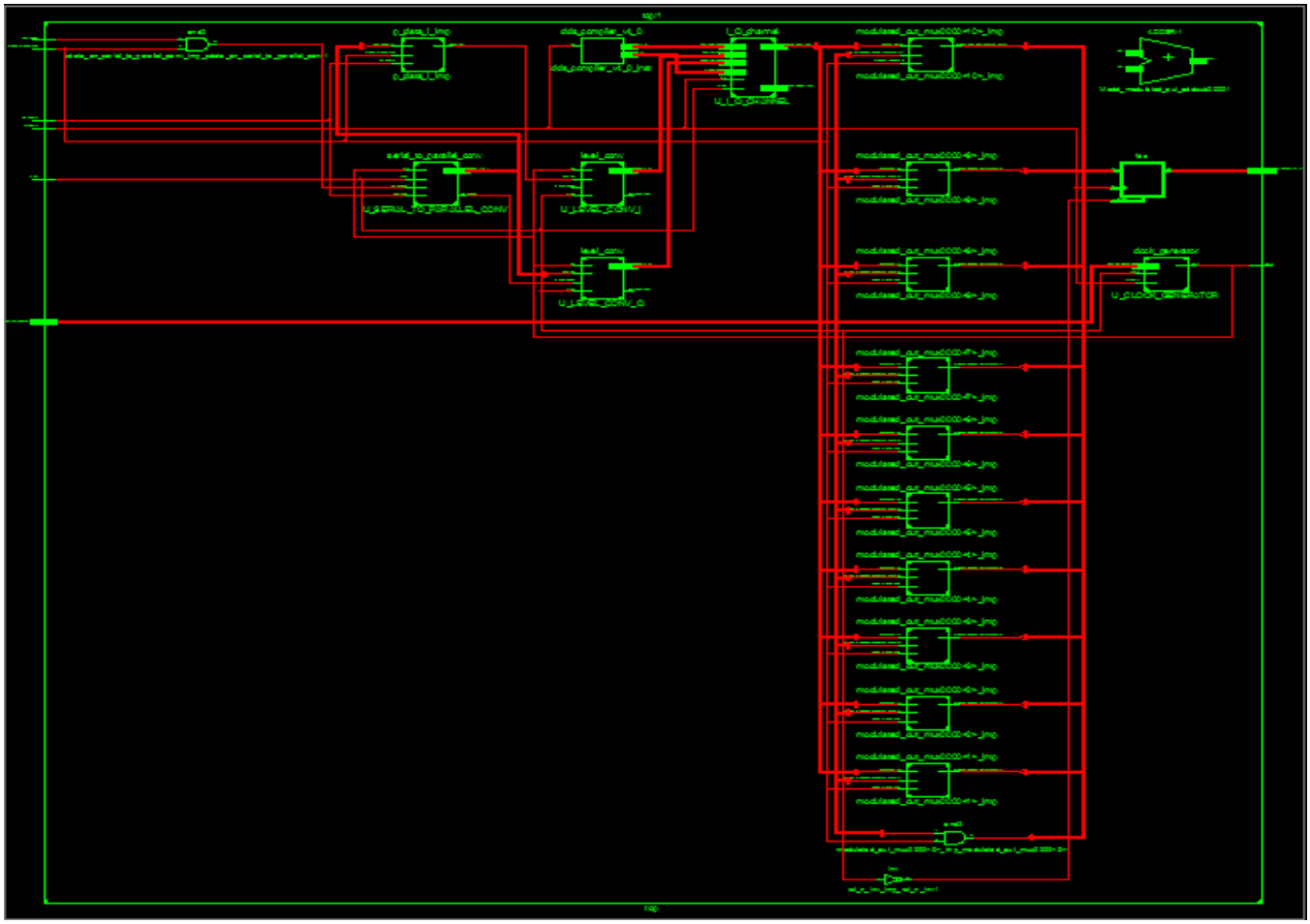

**Figure 10: RTL Schematic for proposed modulation method 1**

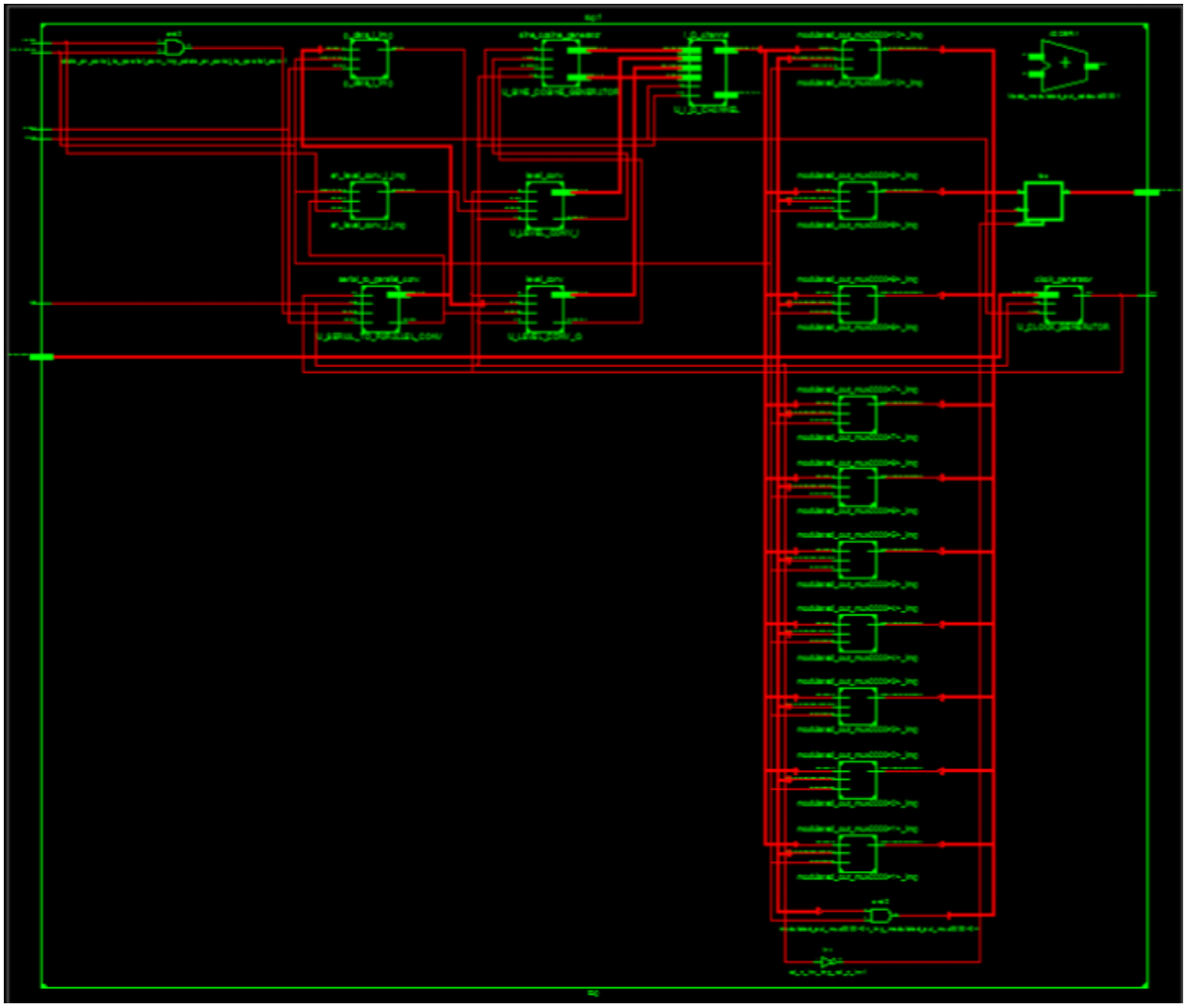

**Figure 11: RTL Schematic for proposed modulation method 2**

## 5. RESULT

The modulator was coded in Verilog HDL and was implemented on Spartan-3E FPGA with all the two above designs. The Xilinx synthesis tool which generates synthesis report mentioning the area utilized by the entire implementation of both design is described in Table 2. Timing report of both design is described in Table 3.

**Table 2 : Area Report**

| **Logic Utilization of xc3s50-pq208** | **Available** | **Proposed Modulation Method 2** | | **Proposed Modulation Method 1** | |
|---|---|---|---|---|---|
| | | **Used** | **% Utilization** | **Used** | **% Utilization** |
| Number of Slice Flip Flops | 1,536 | 80 | 5% | 66 | 4% |
| Number of 4 input LUTs | 1,536 | 112 | 7% | 63 | 4% |
| Number of occupied Slices | 768 | 66 | 8% | 48 | 6% |
| Number of Slices containing only related logic | 66 | 66 | 100% | 48 | 100% |
| Number of Slices containing unrelated logic | 66 | 0 | 0% | 0 | 0% |
| Total Number of 4 input LUTs | 1,536 | 112 | 7% | 79 | 5% |
| Number of bonded IOBs | 124 | 19 | 15% | 19 | 15% |
| Number of BUFGMUXs | 8 | 1 | 12% | 1 | 12% |
| Average Fan out of Non-Clock Nets | | 3.88 | | 2.44 | |
| Number of RAMB16s | 4 | 0 | | 1 | 25% |

**Table 3 : Timing Report**

| Timing Summary | Proposed Modulation Method 2 | Proposed Modulation Method 1 |
|---|---|---|
| Min period | 4.386ns | 5.301ns |
| Max Frequency | 228MHz | 189MHz |

## 6. CONCLUSION

The proposed QPSK modulator1 used Xilinx's soft IP DDS. While the proposed QPSK modulator 2 has ROM based approach & hence does not use multiplier, adder, sub tractor. From area report it is observed the proposed QPSK modulator1 utilized considerably less area compare to the proposed QPSK modulator2, but from timing report it is observed as high throughput is achieved by the proposed QPSK modulator2. We can conclude as proposed modulation method 1 occupied less area but proposed modulation method 2 works on comparatively higher speed. The future scope of the idea is to estimate power of both modulation methods. It is expected as proposed QPSK modulator1 will consume less power than proposed QPSK modulator2 due to area factor.

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