# Design and Implementation of Low Power 32 Bit Arithmetic Logic Unit

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## ABSTRACT
This paper presents the construction of 32-bit ALU (Arithmetic Logical Unit) using VHDL. The main intention to design 32 bit ALU to defeat the area and power of the design. Which is a digital circuit that executes Arithmetic Logic Unit. ALU is a fundamental building block of the central processing unit (CPU) of a computer, and even the simplest microprocessors contain one for purposes such as maintaining timers. The coding will be written in VHDL and verified in I-Sim. After the coding the synthesis of the code was performed using Xilinx-ISE. Synthesis tool ISE 14.7. The ALU executes the desired operation and generates the result consequently. This designed put away very less area and only 193 LUTs occupy out of 10944 LUTs.

## Keywords
ALU, 32 bit Logic Unit, Shifter. Adder, logic unit, shift unit**.**

## 1. INTRODUCTION
To design a 32 bit Arithmetic Logic Unit, which is a digital circuit that execute arithmetic and logical operations using VHDL. The ALU is a fundamental building block of the central processing unit (CPU) of a computer, and even the simplest Microprocessors contain one for purposes Such as maintaining timers. The processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs; a single component may contain a number of ALUs.

Mathematician John von Neumann proposed the ALU conception in 1945, Research into ALUs remains an significant part of computer science, falling under Arithmetic and logic structures in the ACM Computing Classification System Here, ALU is designed using VHDL (VHSIC hardware description language) is a hardware description language used in electronic design automation to explain digital and mixed signal systems such as field-programmable gate arrays and integrated circuits.

## 2. FUNCTION OF ALU
When designing the ALU we will follow the principle "Divide and conquer" in order to use modular design that consists of smaller, more manageable blocks, some of which can be re-used. Instead of Designing the 32-bit ALU as one circuit we will first design one bit adder, Subtractor, OR, AND, NOT, XOR, Left Shift, Right Shift Unit. These bit-slices can then be put together to make a 32-bit Adder, Subtractor, OR, AND, NOT, XOR,, Left Shift, Right Shift Unit. 32-bit Arithmetic Unit an Arithmetic unit does the following task: Addition, Addition with carry, Subtraction, Subtraction with borrows Decrement, Increment and Transfer function. Now first required to design various logic to perform 32 bit ALU function start with making one bit.

## 3. PROPOSED METHOD
The main intention to graph the project is to design a 32 bit Arithmetic Logic Unit which is a digital circuit that performs arithmetic and logical operations using VHDL. The ALU is a fundamental building block of the central processing unit (CPU) of a computer, and even the simplest microprocessors included one for purposes such as maintaining timers. a single component may hold a number of ALUs in this development have designed 32-Bit Arithmetic ,Unit 32-Bit Logic, Unit32-Bit Shifter, Unit 32-Bit Arithmetic And Logical Unit in single unit .shown in fig 1.

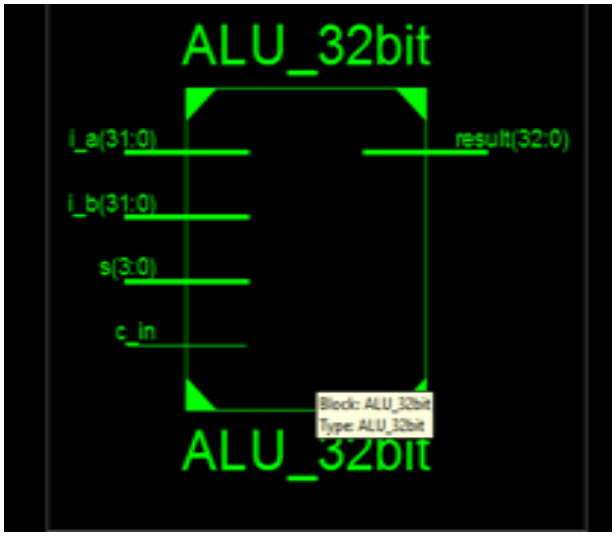


**Fig 1: Block diagram of ALU**

## 4. 32-BIT ARITHMETIC UNIT
An arithmetic unit does the following task: Addition, Addition with carry, Subtraction, Subtraction with borrow, Decrement, Increment and Transfer function [2] shown in fig 2

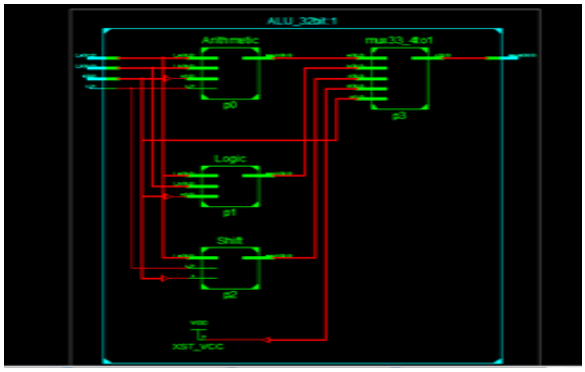


**Fig 2: Block diagram of 32-bit Arithmetic Unit**

## 5. 32-BIT LOGIC UNIT

A Logic unit does the following task: Logical AND, Logical OR, Logical XOR and Logical NOT operation. The design a logic unit that can perform the four basic logic micro-operations: OR, AND, XOR and Complement, because from these four micro-operations, all other logic micro-operations can be derived as shown in fig 3.

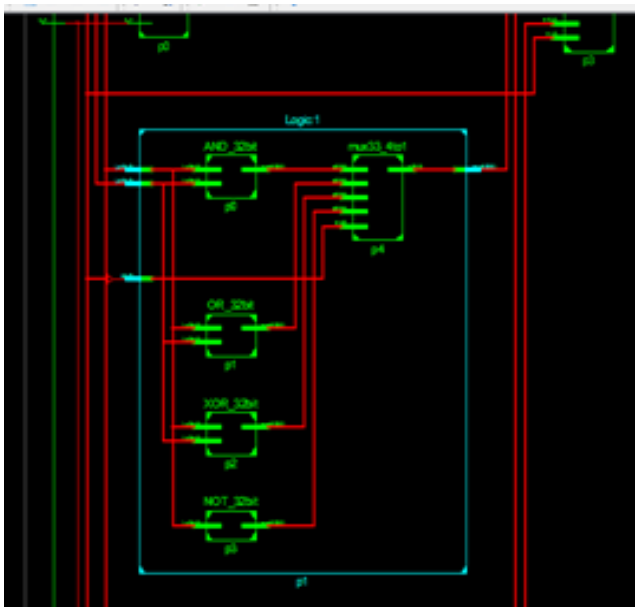


**Fig 3: block diagram of 32-bit Arithmetic Unit**

## 6. 32-BIT SHIFTER UNITS

Shifter unit is used to perform logical shift micro-operation. The shifting of bits of a register can be in either direction- left or right. A combinational shifter unit can be constructed as shown in fig 4. Shifter unit is used to perform logical shift micro-operation. The shifting of bits of a register can be in either direction- left or right.

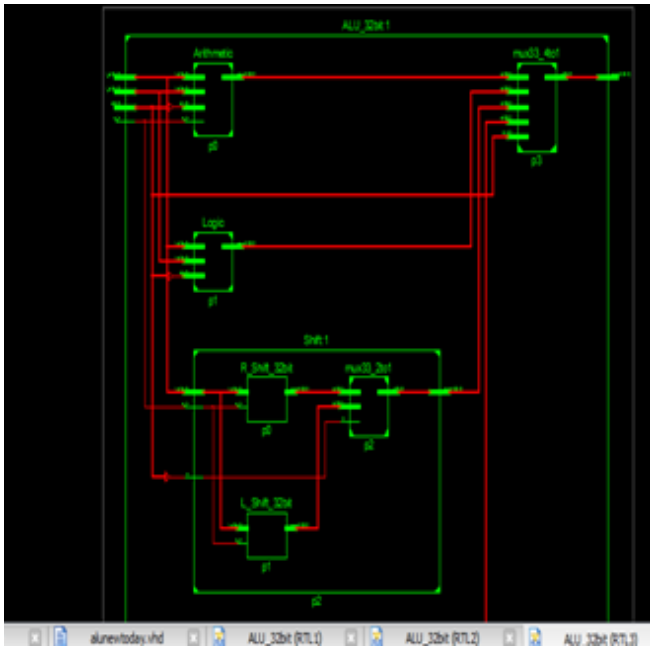


**Fig 4: block diagram of 32-bit Arithmetic Unit**

## 7. 32-BIT ARITHMETIC AND LOGICAL UNIT

The approach used here is to split the ALU into three modules, 1 arithmetic, 1 logic and 1 shift module. The arithmetic, logic and shifter units introduced earlier can be combined into ALU with common selection lines. The shift micro-operations are often performed in a separate unit, but sometimes the shifter unit made part of overall ALU. As shown in fig 5.

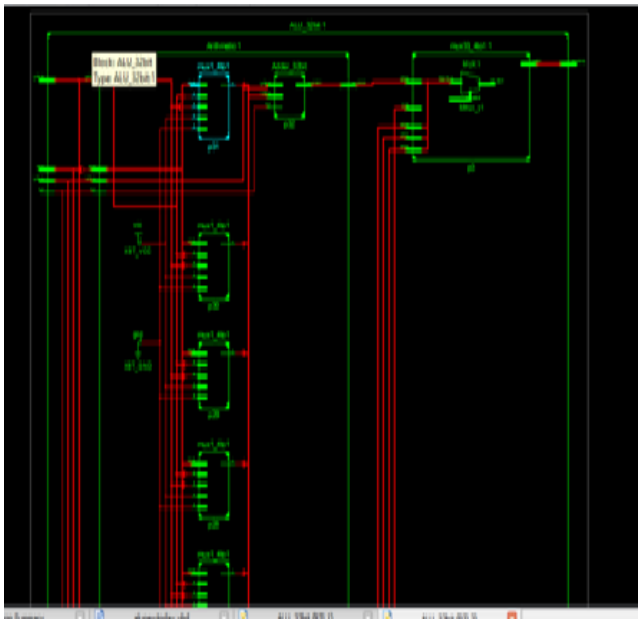

**Fig 5: Block diagram of 32-bit Arithmetic Unit**

| ALU_32bit Project Status (09/04/2016 - 13:40:35) | | | |
|---|---|---|---|
| Project File: | alunewtoday.xise | Parser Errors: | No Errors |
| Module Name: | ALU_32bit | Implementation State: | Programming File Generated |
| Target Device: | xc4vfx12-10sf363 | • Errors: | No Errors |
| Product Version: | ISE 14.1 | • Warnings: | 1 Warning (0 new) |
| Design Goal: | Balanced | • Routing Results: | All Signals Completely Routed |
| Design Strategy: | Xilinx Default (unlocked) | • Timing Constraints: | |
| Environment: | System Settings | • Final Timing Score: | 0 (Timing Report) |

| Device Utilization Summary | | | | |
|---|---|---|---|---|
| Logic Utilization | Used | Available | Utilization | Note(s) |
| Number of 4 input LUTs | 193 | 10,944 | 1% | |
| Number of occupied Slices | 105 | 5,472 | 1% | |
| Number of Slices containing only related logic | 105 | 105 | 100% | |
| Number of Slices containing unrelated logic | 0 | 105 | 0% | |
| Total Number of 4 input LUTs | 193 | 10,944 | 1% | |
| Number of bonded IOBs | 102 | 240 | 42% | |
| Average Fanout of Non-Clock Nets | 3.07 | | | |

**Fig 6: Synthesis report of 32-bit Arithmetic Unit**

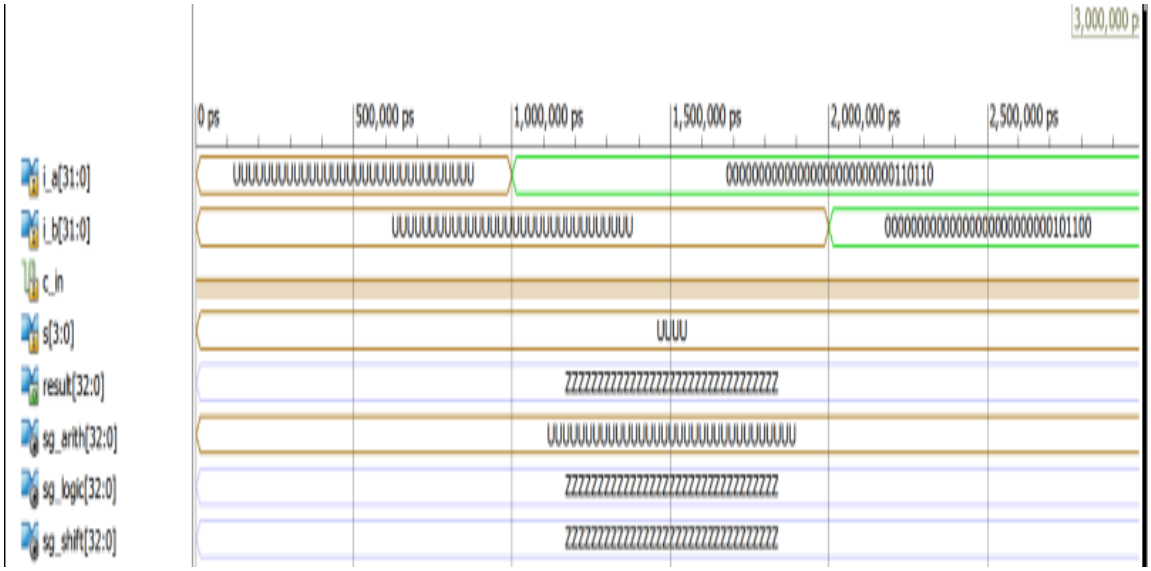


**Fig 7: simulation view of 32-bit Arithmetic Unit**


**Figure .8 Simulation view of 32-bit Arithmetic Unit**

The process of generating a logic circuit from an initial specification is called synthesis that may be given in the form of diagram or code written in the hardware description language which means an abstract form of desired circuit behavior. Typically, it represents the register transfer level (RTL) and is rotate into a design accomplishment in term of logic gates as shown in fig 6.

## 8. SIMULATION & RESULT

In this work, Xilinx and I-sim tools are used for timing analysis and Synthesis. The simulation output for both 32-bit ALU is presented. After verifying the block diagram, the behavior of 32-bit ALU is checked by simulation process as shown in fig 7 and fig 8.

**Table 1: Comparison between previous & proposed system**

| Design | Delay (Ns) | PDP W*ps | Power [Nw] |
|---|---|---|---|
| **Previous Design [1]** | 89.62 | 2957 | 33 |
| **Proposed design** | Delay: 33.468 ns (Levels of Logic = 37) | 5.555 | 0.166 |

## 9. CONCLUSIONS

Using VHDL, we have designed a 32 bit ALU, which can execute the various arithmetic operations like Addition, Subtraction, Increment, Decrement, Transfer, logical operations such as AND, OR, XOR, NOT and also the shift operation. This area proficient adder put away very less area about 1% and only 193 LUTs used out of 10944 .Here the RTL coding is done first using a VHDL and simulation is will be carried out by using I-SIM 14.1. These area-competent applications.

By introducing operation of ALU better performance is acquire in terms of area. This work can be extended for the apprehension of the 128-Bit ALU and there is an extent for VLSI relevance.

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## 11. AUTHOR PROFILE

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