Abstract

The main objective to design this paper to increasing importance of commercial application, economic and Internet-based applications the decimal adder provide useful statistic in formative each adder's performance and scalability. There is a new interest in providing hardware support to handle decimal data. In this paper, a new architecture binary to BCD converter for multi-operand addition implement of binary coded decimal (BCD) operands, which is the core of high speed multi-operand adders. The proposed Simulation results show that the add-3 digit BCD adder achieves an improvement of 70% in delay and area and it consume very less power. The 2,4,8,16-digit BCD look-ahead adder shown to achieve at least 90% faster than the accessible ripple carry one. The coding will be written in VHDL and verified in I-Sim. After the coding the synthesis of the code was performed using Xilinx-ISE. Synthesis tool ISE 14.7.

References

1. Area-Efficient and Power-Efficient Binary coded decimal Converters Sri Rathan
Index Terms

Computer Science
Circuits and Systems

Keywords

BCD adder, add-3 algorithm, binary to BCD converter, decimal arithmetic.