Low Power Dissipation Binary to BCD Converter for Multi-Operand B/D Adder

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ABSTRACT
The main objective to design this paper to increasing importance of commercial application , economic and Internet-based applications the decimal adder provide useful statistic in formative each adder's performance and scalability. There is a new interest in providing hardware support to handle decimal data. In this paper, a new architecture binary to BCD converter for multi-operand addition implement of binary coded decimal (BCD) operands, which is the core of high speed multi-operand adders. the proposed Simulation results show that the add-3 digit BCD adder achieves an improvement of 70 % in delay and area and it consume very less power. The 2,4,8,16-digit BCD look-ahead adder shown to achieve at least 90 % faster than the accessible ripple carry one. The coding will be written in VHDL and verified in I-Sim. After the coding the synthesis of the code was performed using Xilinx-ISE. Synthesis tool ISE 14.7.

Keywords
BCD adder, add-3 algorithm, binary to BCD converter, decimal arithmetic.

1. INTRODUCTION
The utilization of decimal arithmetic has been growing over binary due to increase in the applications of internet banking and there are a lot of places where accuracy is very important factor. Binary digits have a drawback of not being capable to represent digits approximating 0.1 or 0.7, necessitate an infinitely frequently binary number. The accessibility of multi-operand decimal adders can be facilitating financial and commercial applications based on existing massive databases. The simultaneous addition of numerous decimal numbers is the ordinary operation in multiplication and division algorithms. Multi-operand addition is a very important operation as it is a core element of arithmetic operations, for instance division and Multiplication. In case of decimal multiplication Multi-operand decimal addition comes In Useful large amounts of decimal data This paper bring in a multi-operand decimal Addition circuit, which speeds up the process of decimal addition. And providing hardware support in this direction is henceforth necessary. Improving BCD architectures to enable faster and compact arithmetic.

In this paper we introduce a new architecture for binary to BCD Conversion for multi-operand adder .which forms the core of decimal multiplication algorithms such as [7]. The speedup, area decrease and power utilization of the proposed architecture is analyzed and comparisons through existing architectures is provided. The Results show that the proposed design brings considerable enhancement in terms of latency, area and power consumption overview on common BCD conversion and it's require.

2. PROPOSED LOGIC
The main purpose of the proposed is to achieved vary greatly accomplished fixed bit binary to Binary Coded Decimal (BCD) conversion in expression of power and area. As mentioned previous, most of the newly proposed adder use 16-bit binary to Binary Coded Decimal (BCD) converters.

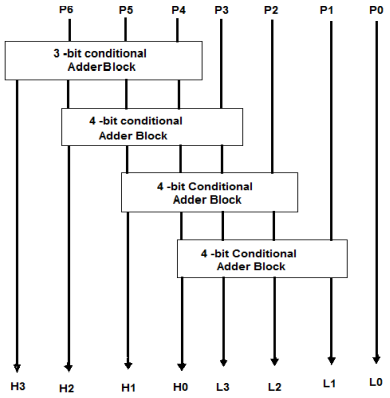

Fig .1 BCD to Binary Conversion

The planned design has been purposely designed for such converters. Though the shifting and adding by 3 algorithms is not novel, the architecture execution by means of adding by constant which ultimately makes it area efficient is given away in fig.1. This paper focuses on the design and synthesis of efficient binary to decimal architecture for high performance decimal adder based on add-3 algorithm [1].

	Hundreth BCD	Tens BCD	Ones BCD	8-bit binary	
Original binary number				0111	1100
Shift left three times no adjust			011	1110	0
Shift left Ones = 7, ≥5			0111	1100	
Add 3			1010	1100	
Shift left Ones = 5		1	0101	100	
Add 3		1	1000	100	
Shift left 2 times Tens = 6, ≥5		110	0010	0	
Add 3		1001	0010	0	
Shift left BCD value is correct	1	0010	0100		

Fig .2 BCD to Binary Conversion

The solution idea following the algorithm can be unstated as follow:-

1. Each one times the number is shifted left; it is multiplied by 2 as it is change to the BCD position

2. The value inside the BCD digits are the similar as binary till 9 binary number or lower than 9 binary number . Though if it is 10 or higher than it is not correct BCD number because for BCD, this should carry over to the after that digit. A improvement have to be needed and this can be made through adding 6 to this binary digit.

3. The simplest approach to do this is to distinguish if the value inside the BCD digit locations are 5 or above previous to the shift (i.e. X2). If it is ≥5, then add 3 to the value (i.e. adjust by +6 after the shift).

4. The hardware to achieve binary toward BCD conversion is shown below. Shifting is simple – just wiring all signals one location to the left. For every one of the BCD locations, we need an "adjust" module which execute and go behind operation: if the value is ≥5, then add 3. This is best illustrated using our example.

3. ANALYSIS & IMPLEMENTATION

Once the all VHDL modules are prepared, they should be simulated before they are put in actual hardware chip. We can generate a test counter waveform from the Project New Source menu of ISE and it will support in setting up the simulation. Once we simulate our design and feel it is function properly, then we can move on to generating the data needed to essentially program the objective tool with our system design [6].

4. ADDER IMPLEMENTATION

Execution of 16 bit Binary to Binary coded decimal Converter adder using add -3-addition RCA has been done using Xilinx 14.1 and simulator has commend out by l-Sim 14.1e tool.

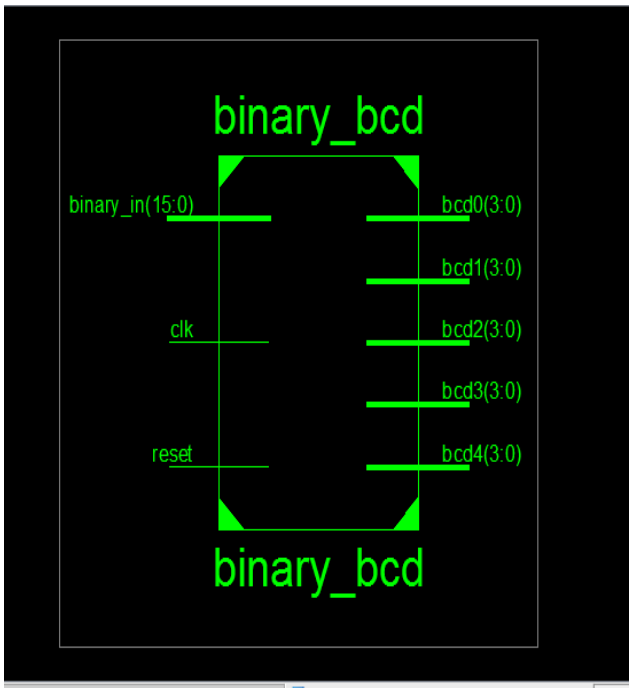

Fig .3 Block Diagram of 16 bit Binary coded decimal Converter

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Total Number Slice Registers	109	10,944	1%	
Number used as Flip Flops	65			
Number used as Latches	44			
Number of 4 input LUTs	56	10,944	1%	
Number of occupied Slices	63	5,472	1%	
Number of Slices containing only related logic	63	63	100%	
Number of Slices containing unrelated logic	0	63	0%	
Total Number of 4 input LUTs	56	10,944	1%	
Number of bonded IOBs	38	240	15%	
Number of BUFG/BUFGCTRLs	2	32	6%	
Number used as BUFGs	2			

Fig .4 Synthesis report of 16 bit Binary coded decimal Converter

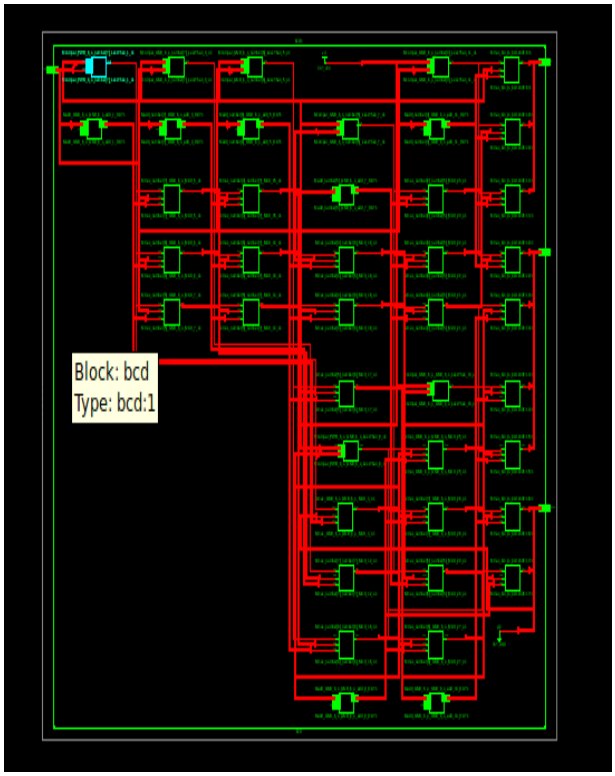

Fig .5 RTL View of 16 bit Binary coded decimal Converter

Binary in, clk, rst are inputs which are going to (N-1 downto 0) bcd0, bcd1, bcd2, bcd3, bcd4: are outputs show in Fig 6.1 RTL view of 16 bit binary coded decimal converter and fig 5 represnts the various combination of multiplexer and flip flop and i/o lines of related to LUTs show in Fig. 6 Binary coded decimal Input Output View RTL View

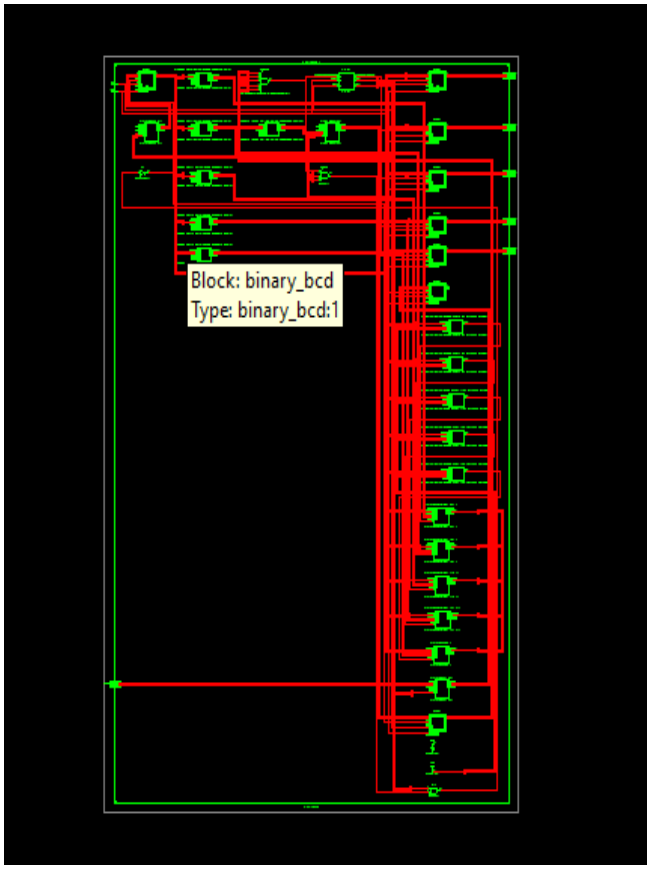

Fig .6. RTL View of 16 bit Binary coded decimal Converter

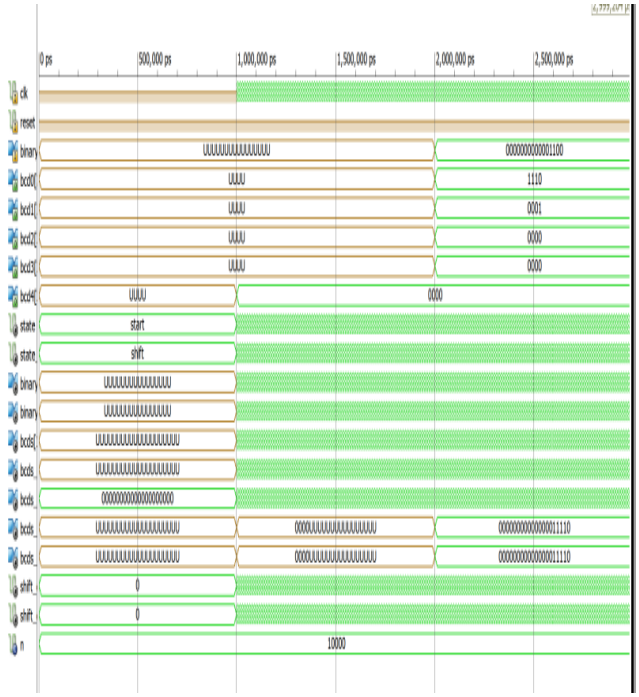

Fig .7 Simulation Result of 16 Bit Binary to BCD Converter

5. SIMULATION RESULT

The Xilinx ISE system is an combine part of design surroundings so as to consists of a locate of programs to generate (capture).

replicate and implement digital intend fig7 show simulation result of binary coded decimal converter which show clock , reset and binary_ in as a input and bcd0,bcd1,bcd2,bcd3,bcd4 as output .-inputs were set to have a clock rate of 100%. Binary to BCD

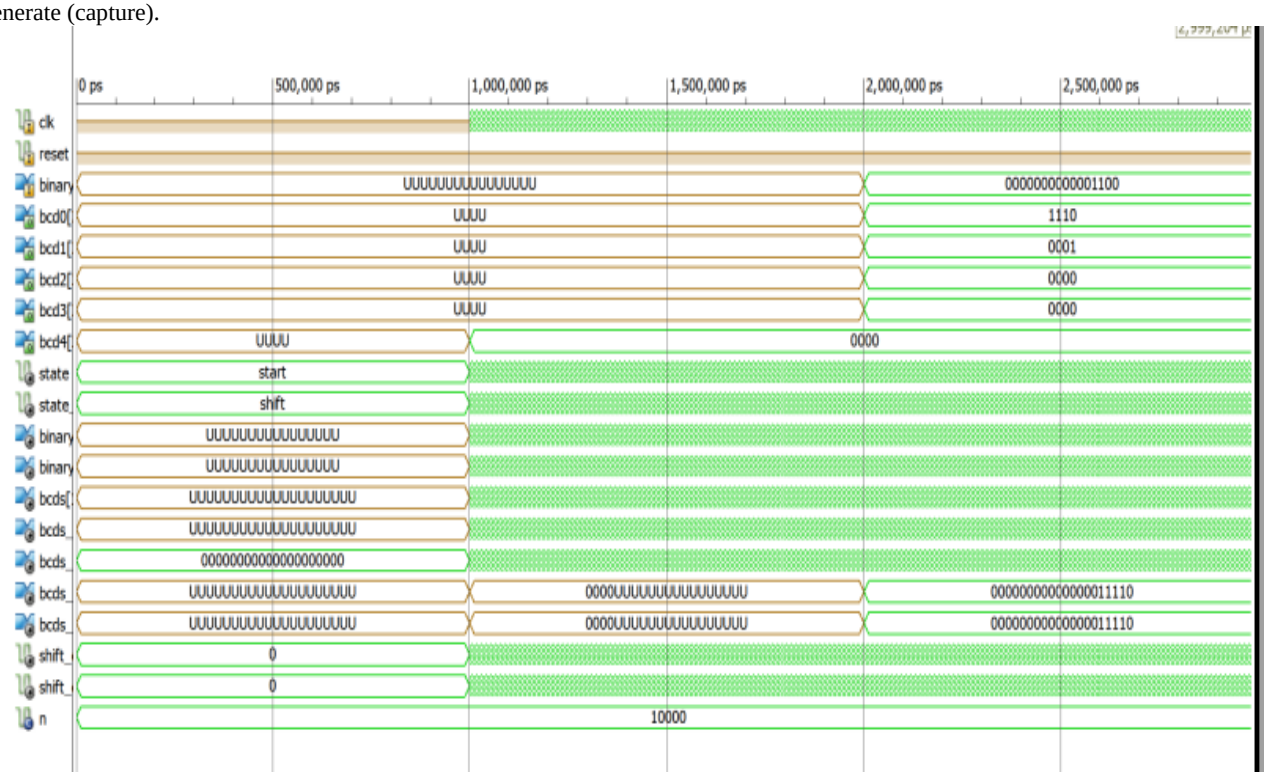

Fig .8 Simulation result of 16 bit binary to BCD converter

Fig.9 Power of 16 bit binary to BCD converter

Table 1 Comparison table

Design	Delay (Ns)	PDP W*ps	Power [Nw]
Design [1]	1.89	549	549
Proposed design	1.493	0.173	0.173

6. CONCLUSIONS

The comparison of Binary coded decimal converter with existing design [1]. Synthesis results demonstrate that present is a reduction in power and area. This in turn reduces power delay product and Minimum period: 1.493ns (Maximum Frequency: 669.658MHz), Minimum input arrival time before clock: 1.705ns, Maximum output required time after clock: 4.624ns, Maximum combinational path delay: No path found, total power dissipation 0.173 W and total 109 LUTs used out of 10944. Number of Slices 63 out of 5472 number of 4 inputs LUTs Number of bonded IOBs 38 out of 240. In the prospect the majority of the computers will support hardware & software implementation of binary arithmetic's and their logic unit.

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