Design of Booth Multiplier using Double Gate MOSFET

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ABSTRACT
Double gate MOSFET technology is used wherever low power delay product is desired. It uses to reduce leakage current drain induced barrier lowering effect (DIBL) and other short channel affects. In this work 8×8, Booth Multiplier is analysed in 90nm technology, with one single-gate MOSFET technology and then other using the proposed that is Double-Gate MOSFET technique. Depending on the input patterns, the proposed technique saves 24% in power consumption has observed in proposed circuit. Design and simulations are performed in cadence virtuoso and spectre tools using 90nm technology.

Keywords
Booth Multiplier, Double Gate, Low power, Power Delay Product (PDP)

1. INTRODUCTION
In digital signal processing and various applications, multipliers [1] plays an important role. In advance technology many researchers tried to design multipliers which offer the following specifications such as high speed, low power consumption or less power.

Booth algorithm [2] was invented by Andrew Donald in 1950 while study on crystallography at brickbeck college, Bloomsbury London. Booth used reception desk calculators that shifts faster than adding and formed the algorithm to increasing the speed. Booth multiplication involves two techniques to reduce the delay

1. To reduce the number of partial products.
2. To increase the speed at which partial products are added.

Figure 1.1 shows the architecture [3] of booth multiplier . Radix-2 booth multiplier consists 4 logic blocks namely booth encoder is used for encoding multiplier bits and reduce the number of partial products. Partial product generator is used to generate partial products. (9:4,7:3 & 4:2) compressor adder is used for collecting all the partial products and produce the sum and carry vectors.6T-Transistors adder is to produce final product terms.

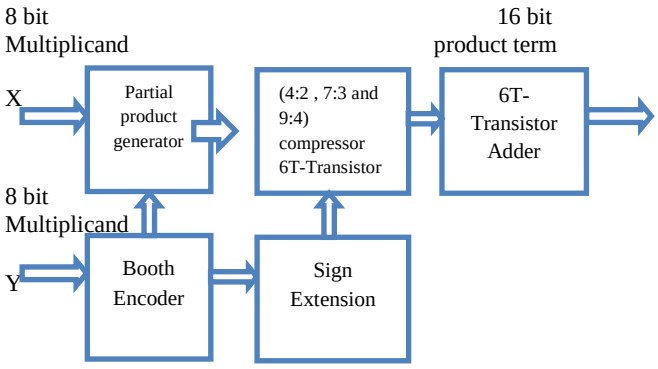

Figure 1.1 Architecture of Booth Multiplier.

2. LITERATURE REVIEW
The need of designing low power VLSI circuits has been increased abundantly and increase demand of portable device like cellular and mobiles. Further increase more number of devices on chip, scaling of device size is required. Number of problems are facing in scaling of bulk MOSFETS. The problems like leakage current, drain induced barrier effect (DIBL) and other short channel affects (SCE'S) degrade the performance of circuits. Design all the blocks of booth multiplier in both single gate and double gate technique. The proposed double gate technique give better performance compare to single gate MOSFET technique.

3. DOUBLE GATE MOSFET TECHNIQUE
Double gate MOSFET [4] technique proposed in 1980. It is used in ultralow power design. DG MOSFETS has drain, source and two gates. The two gates (front & back) electrically coupled together in double gate devices. It reduces has better control over channel conductance and immunity to SCE'S and reduce sub threshold leakage. It operates in two modes such as symmetrical driven (SDDG) and independent driven (IDDG) double gate MOSFET. The below figure 3.1 and 3.2 shows the symbol of double gate MOSFETS and symmetrical mode operation of double gate MOSFETS.

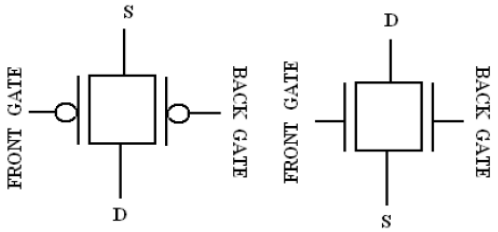

Figure 3.1 circuit symbols for p-type and n-type of Double Gate MOSFETS.

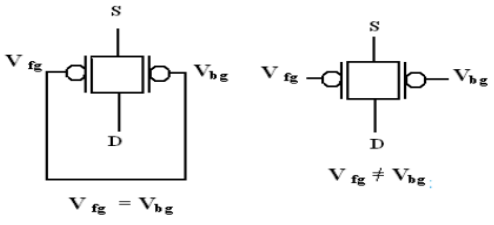

Figure 3.2 symmetrical and independent driven Double Gate MOSFETS.

3.1. General Double Gate operation
The voltage applied on the gate terminals controls the electric field, determining the amount of current flow through the channel.

The most common operations is to switch both gates simultaneously.

Another mode is to switch only one gate & apply a bias to the second gate this is called ground plane (GP) or back gate (BG). The below figure 3.3 shows the schematic diagram of double gate.

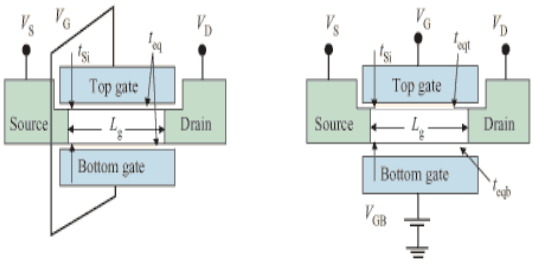

Figure 3.3 Schematic diagram of Double gate.

4. MULTIPIER DESIGN

Multiplier consists 4 logic blocks namely (a) booth encoder is used for encoding multiplier bits and reduce the number of partial products. (b) Partial product generator is used to generate partial products. (c) [4:2, 7:3 & 9:4] compressor 6T-Transistors adder is for collecting all the partial products and produce the sum and the carry vectors. (d) 6T-Transistor adder is to produce final product terms; multiplier architecture is shown in figure1.1. 8×8 multiplier is designed in both single and double gate techniques.

4.1. Booth Encoder

Booth Encoder [5] block that scans 3 bit input from multiplier y and encodes into one of three outputs namely TWO, ONE, NEG. the logic circuit can be easily constructed with the help of truth table 4.1 given below. Figure 4.1 shows the logic circuit of booth encoder is designed in both single and double gate techniques.

Table 4.1 Encoding of Radix-2 Booth Multiplier

Y_j+1	Y_j	Y_j-1	Zero	Two	One	Neg	Partial Products
0	0	0	1	1	0	0	0
0	0	1	1	0	1	0	1×multiplicand
0	1	0	0	0	1	0	1×multiplicand
0	1	1	0	1	0	0	2×multiplicand
1	0	0	0	1	0	1	-2×multiplicand
1	0	1	0	0	1	1	-1×multiplicand
1	1	0	1	0	1	1	-1×multiplicand
1	1	1	1	1	0	1	0

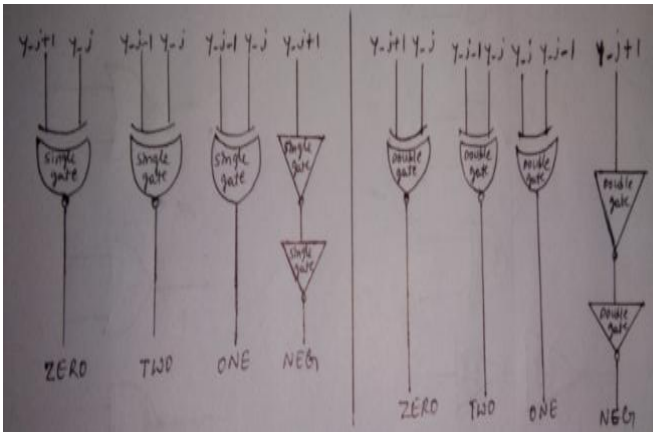

Figure 4.1 Booth Encoder Blocks in both Single & Double gate designs.

4.2. Partial Product Generator Block (PPG)

Based on the output of booth encoder block in the ppg block [6] with select either X_j or X_j-1 and produce complement depending upon NEG value. Figure 4.2.1 shows the logic diagram of ppg block is designed in both single and double gate techniques. Multiplication is achieved by shifting the bit by bit one position towards left and negation by taking two's complement it. Since there are 5 encoders & 40 ppg blocks required to design 8×8 booth multiplier. Figure 4.2.2 shows partial products are generated using booth encoder and partial product generator block. Figure 4.2.3 shows generation of partial product using MBE method.

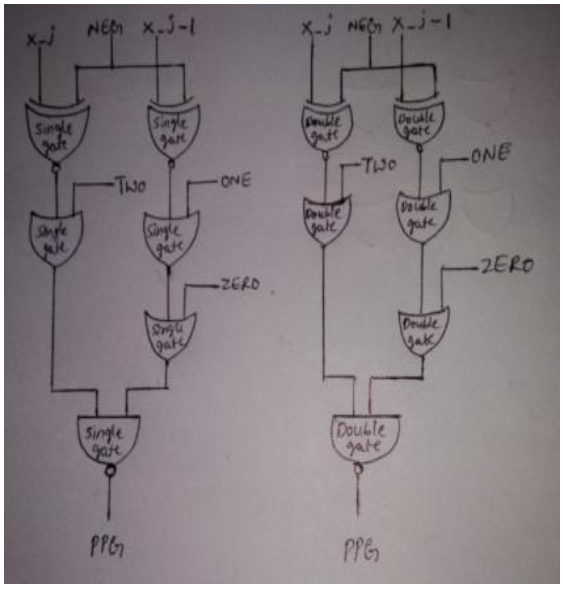

Figure 4.2.1 Partial product generator block in both designs.

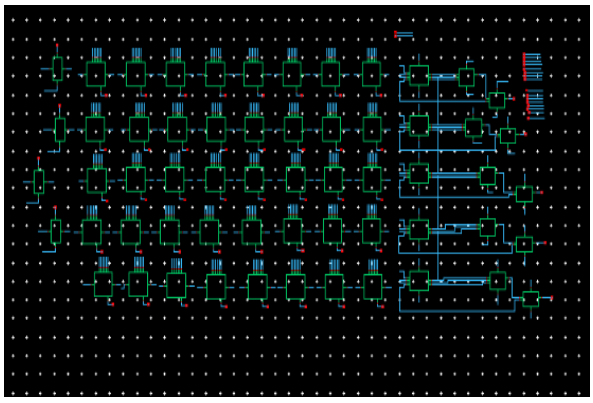

Figure 4.2.2 Architecture of 8×8 Booth Encoder and Partial product genertor block.

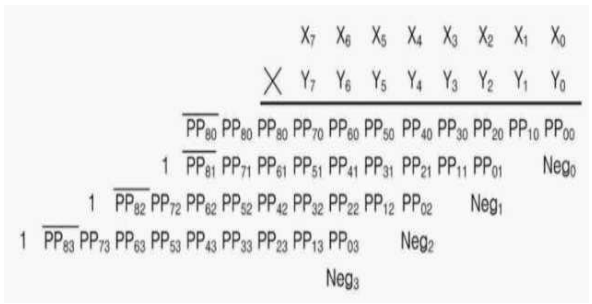

Figure 4.2.3 Generation of partial product using MBE method.

4.3. Compressor [4:2, 7:3 & 9:4] 6T-Transistors Adder

A compressor adder block is used to add the partial products that were produced in PPG module. In PPG module 4:2 takes (in1, in2, in3, in4 & cin) produce outputs (sum, cout1, cout2). 7:3 compressor takes (in1, in2, in3, in4, in5, in6, in7 & cin) produce outputs (sum, cout1, cout2, cout3). 9:4 compressor takes (in1, in2, in3, in4, in5, in6, in7, in8, in9 & cin) produce outputs (sum, cout1, cout2, cout3, cout4). This block is used to add more carry's with partial product values, cin comes from previous stage and will act as cin of next stages. It is designed using both single and double gate techniques. Figure 4.3.1, 4.3.2 and 4.3.3 shows diagram of 4:2, 7:3 & 9:4 compressor adder.

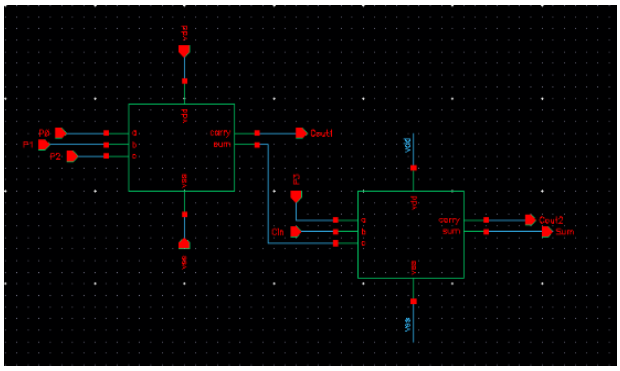

Figure 4.3.1 Compressor 4:2 Adder

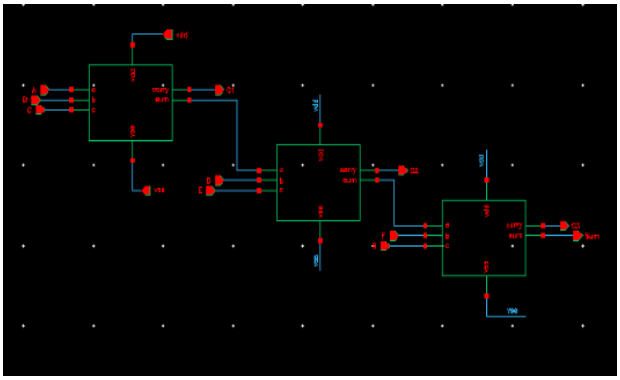

Figure 4.3.2 Compressor 7:3 Adder

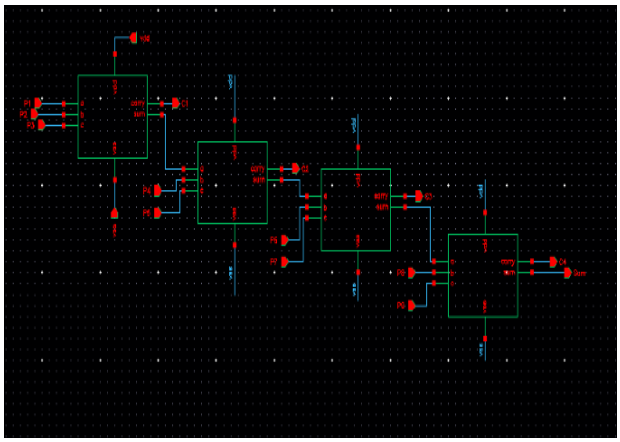

Figure 4.3.3 Compressor 9:4 Adder

4.4. 6T-Transistors Adder

6T-Transistors of one bit full adder [7] is designed by transmission gate in both single and double gate techniques. It generates sum and carry vectors of 16 bit each, sum and carry vectors finally added with the help of 16 bit adder to produce final 16 bit product terms. It is shown in figure 4.4.1 and 4.4.2 designed in both gate techniques. It has less transistors and consumes less area.

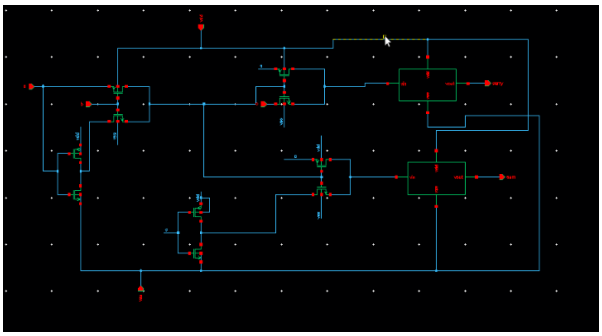

Figure 4.4.1 Design of single gate based 6T-Transistors Adder

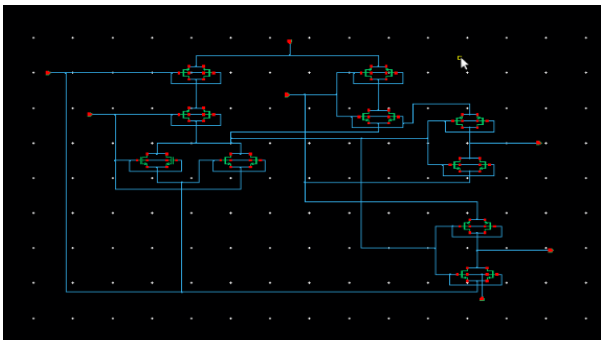

Figure 4.4.2 Design of Double gate based 6T-Transistors Adder

4.5. Complete Architecture of Booth Multiplier

Combine all the blocks according to the architecture of booth multiplier shown in figure 1.1. figure 4.5.1 and 4.5.2 shows complete architecture of booth multiplier designed in single and double gate techniques.

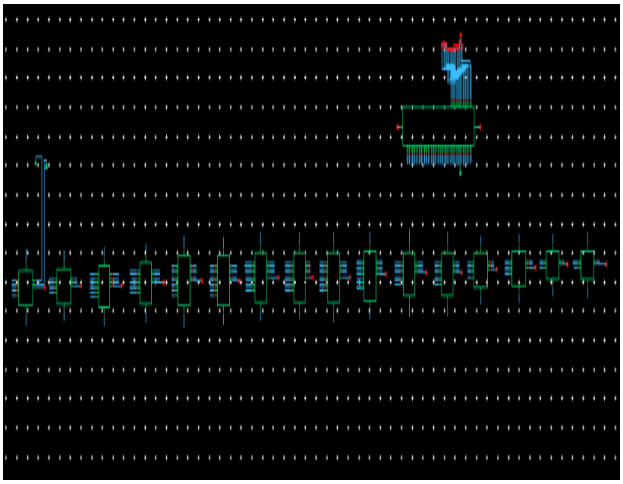

Figure 4.5.1 Single gate based Booth Multiplier.

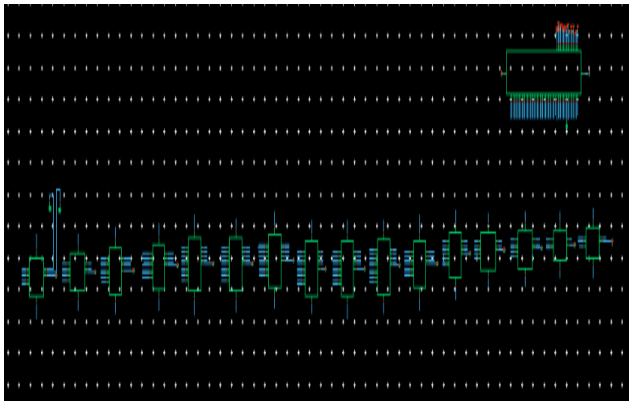

Figure 4.5.2. Double gate based Booth Multiplier

5. RESULTS

All the circuit synthesis & simulation work are performed in cadence virtuoso & spectre tools using 90nm technology. Depending upon the inputs applied the proposed design contributes 24% power reduction compare single gate technique. Table 5.1 shows comparison of power delay product and power of single and double gate techniques.

Table 5.1. Comparison table of power and power delay product (PDP) of Booth Multiplier.

DESIGN	TOTAL POWER (µw)	DELAY (ns)	POWER DELAY PRODUCT
Single Gate	4.923E-3	20.12E-15	0.99 µw/ns
Double Gate	4.84E-3	19.49E-15	0.9401 µw/ns

The transient analysis has been performed for different input voltages with parameters of total power and power delay product proposed in figure 5.1 and 5.2 shown below.

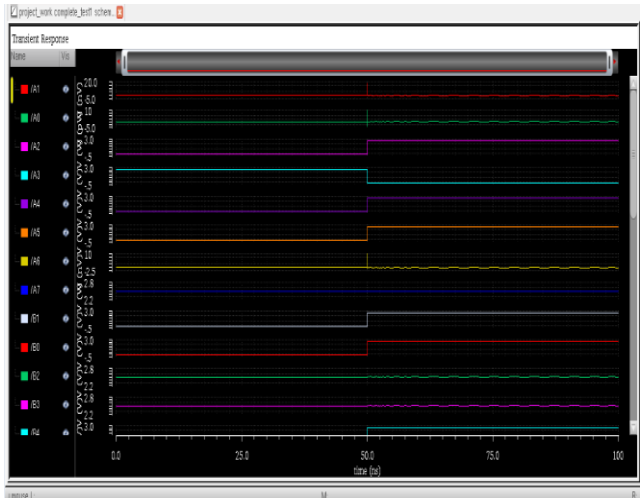

Figure 5.1 simulated output of Booth Multiplier

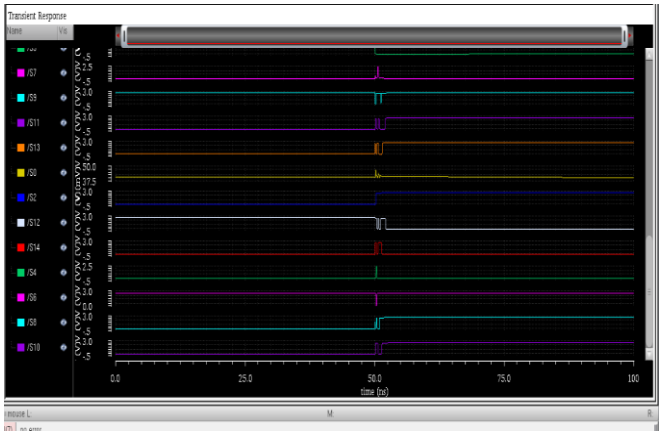

Figure 5.2 simulated output of Booth Multiplier.

The voltage variation of power consumption and power delay product with respect to input voltage. The graph figure 5.3 shows a power consumption compared between single gate and double gate based booth multiplier. This graph revels 24% reduction in power consumption DG MOSFET based booth multiplier.

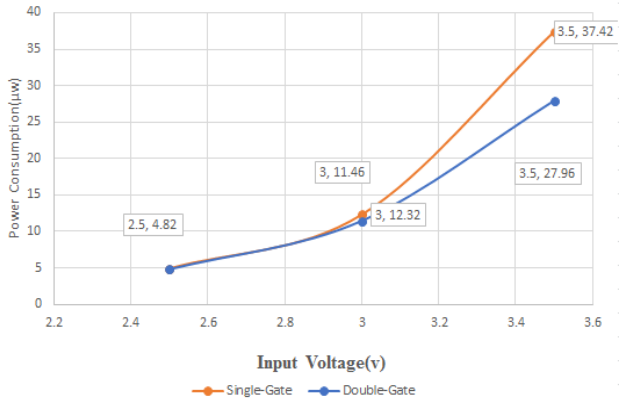

Figure 5.3 Power consumption with input voltage

The below figure 5.4 graph shows comparison between power delay product and with respect to input voltage and it is observed that there is 60% reduction in PDP.

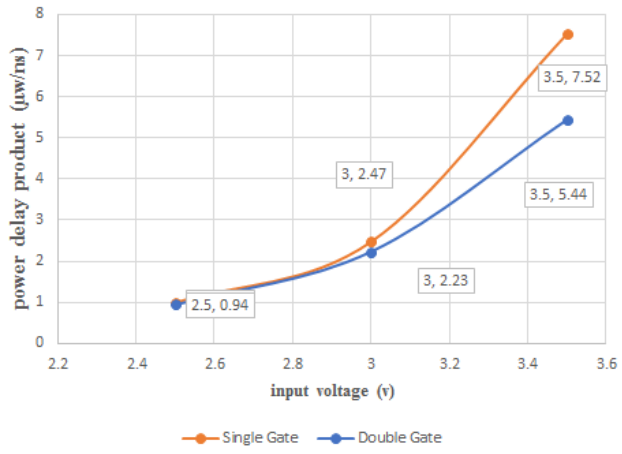

Figure 5.4 Power delay product with input voltage

6. CONCLUSION

The 8bit Booth Multiplier is designed using Double Gate technique by keeping in mind that, the parameters like power and power delay product should be less all the modules are designed using both approach. Using this double gate technique the power consumption is reduced for DG-MOSFET based Booth Multiplier as compared with SG-MOSFET technique. It is observed that the power delay product with input voltage is better for DG-MOSFET based booth multiplier circuit. The proposed circuit has consumes less power and performed higher speed. The proposed circuit can be used in low power design digital signal processors.

7. REFERENCES

[1] J.S. Kim, H.M. Oh; C. W. Byeon; J. H. Son; J. H. Lee; J. Lee; C. Y. Kim, "V-band×8 Frequency Multiplier with optimized structure and high Spectral Purity Using 65-nm CMOS Process" in IEE Microwave and Wireless Components Letters, Vol.PP, no99,pp..1-3.

[2] M. Zamin Ali Khan1, Hussain Saleem2, Shiraz Afzal3 and Jawed Naseem4, "An Efficient 16-Bit Multiplier based on Booth Algorithm", International Journal of Advancements In Research and Technology, Volume1, Issue 6, November-2012 ISSN-2278-7763

[3] M. Singh, A. K. Maurya, S. P. Singh and S. K. Balasubramanin, "6×6 Booth Multiplier Implemented in Modified Split-path data driven dynamic 4 logic," Students Conference on Engineering and Systems, Allahabad, 2014, pp.1-4.

[4] J. K. Sahani and S. Singh, "Design of Full Adder Circuit Using Double Gate MOSFET", 2015 Fifth international Conference on Advanced Computing and Communication Technologies, Harayana 2015 pp.-57-60.

[5] J. L. Beuchat and J. M. Muller "Multiplication algorithms for radix-2 RN-codings and Two's Complement numbers" 2005 IEEE International Conference On Application-Specific Systems, Architecture Processors (ASAP'05), 2005, pp.-303-308.

[6] S. –R. Kuang, J. P. Wang, and C.-Y. Guo, "Modified Booth multipliers with a regular partial product array," IEE Trans. Circuit Syst. II, Exp. Briefs, vol. 56, no. 5, pp.404-408, May 2009.

[7] M. Vesterbacka, "A New six-transistor CMOS XOR Circuits with complementary output," Proc. 42nd Midwest Symp. On Circuits and Systems, Las Cruces, NM, Aug. 1999.