Abstract

The architecture design for statistical operations to compute the Mean, Variance, Standard Deviation, RMS (Root Mean Square), Covariance, and MSE (Mean Square Error) values has been implemented on hardware concerning Xilinx Spartan 3E XC3S500E FPGA and worked properly up to maximum frequency of 73.252 MHz. The practical outcomes have been compared with the theoretical values calculated by Matlab with maximum error of 1.425%. New methods of design were concerned for the architecture of each function to reduce the number of slices.

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**Index Terms**

Computer Science  
Signal Processing

**Keywords**

FPGA, VHDL, Statistical Operations, Accumulators, fixed point.