A New Technique for Leakage Power Reduction in CMOS circuit by using DSM

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Authors:

Chandra Pratap Singh Rathore, Laxmi Kumre

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Abstract

In the continuous scaling down of technology in the field of integrated circuits, low power circuits are in demand for reliability and performance. This research focuses on run time leakage reduction technique for CMOS devices, this work introduces two well-known approaches, stack approach with pass transistor approach for reduction of the leakage power and improves the performance of the circuit. Here NMOS transistor and PMOS transistor parallel to each other in between pull up and pull down network, the resistance is increased by providing stacking of the transistor for mitigation of leakage power. For proper validation and verification of results we use the module of proposed NAND gate to built a Full Adder circuit and for verification of results. Here NMOS pass transistor is connected between pull up network and pull down network similarly PMOS transistor is also connected between pull up network and pull down network both NMOS and PMOS pass transistor are self controlling transistor which reduces the power consumption in active and ideal mode at 43.33%, 43.33%, 86.07% and 86.04% at 25oC respectively as compared with the standard 2 input NOT, AND, NAND and NOR gates. Average dynamic power is reduced to 14.34%, 14.34%, 34.69%, 30.68% respectively.
References

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Keywords

Low Power, Stack approach, Pass Transistor, High Performance