A New Technique for Leakage Power Reduction in CMOS circuit by using DSM

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ABSTRACT
In the continuous scaling down of technology in the field of integrated circuits, low power circuits are in demand for reliability and performance. This research focuses on run time leakage reduction technique for CMOS devices, this work introduces two well known approaches, stack approach with pass transistor approach for reduction of the leakage power and improves the performance of the circuit. Here NMOS transistor and PMOS transistor parallel to each other in between pull up and pull down network, the resistance is increased by providing stacking of the transistor for mitigation of leakage power. For proper validation and verification of results we use the module of proposed NAND gate to built a Full Adder circuit and for verification of results. Here NMOS pass transistor is connected between pull up network and pull down network similarly PMOS transistor is also connected between pull up network and pull down netwotk both NMOS and PMOS pass transistor are self controlling transistor whch reduces the power consumption in active and ideal mode at 43.33%, 43.33%, 86.07% and 86.04% at 25oC respectively as compared with the standard 2 input NOT,AND,NAND and NOR gates. Average dynamic power is reduced to 14.34%, 14.34%, 34.69%, 30.68% respectively.

Keywords
Low Power, Stack approach, Pass Transistor, High Performance

1. INTRODUCTION
Since the advancement of the CMOS technology, increased number of transistors per die with better performance is the main operating feature for the chip manufacturers. The huge competition in semiconductor industry has forced the manufacturers to put more transistors per chip immensely for the economic benefit of semiconductor industry and run towards these goals is increasing exponentially, which is also increased the power dissipation consequently. This excessive consumption of power is dominating factor in chip designing, which adds to short battery life and high chip temperature in various portable electronics devices, hence reduces the operating life of IC (Integrated circuits). In order to increase the performance of the chip and reduces the heating along with high driving capability at lower supply voltage, the VTH is reduced [1, 2]. Scaling of the threshold voltage (VTH) results in exponential increase in subthreshold leakage current (ISUB) as VTH is proportional to ISUB which occur in nano devices [3-4].

Although from many years, silicon based CMOS technology has emerged, it is the most dominant technology for fabrication of transistors to enhance the performance and cost effective VLSI circuits, the revolutionary nature of new systems such as the wired and wireless communication technologies, high performance imaging systems, smart appliances and the like are constantly challenging the boundaries of various technological fronts including silicon CMOS [2].

In very large scale integration circuits, power consumption play important role in CMOS circuit. In nano scale CMOS circuit design there are two types of power consumption static power which flow in when circuit is in ideal condition and dynamic power when circuit has switching. For the decade getting high performance, high packing density and low power reducing the transistor size scaling is required [5]. The technology is continuously and rapidly evolving the production of smaller systems with minimized power dissipation. Scaling of CMOS circuit increases, threshold voltage decreases which results in exponentially increase in sub-threshold leakage current which results in increase of static power dissipation. Due to reducing transistor size, the channel length also become short which increase the leakage current in the transistor in off condition. Leakage power is a very serious problem in mobile application, different type of technique are used at circuit level and process level to resolve this problem[6-9].

This paper is organised as follows in section II, all the reviewers have given their suggestion on leakage power and we have seen as we scale down the technology subthreshold and gate oxide leakage current will dominant. In section III, leakage reduction technique is proposed for mitigation of static power with scaling of technology. In section IV, there is a comparison of different parameters of power consumption at 45nm and 32nm technology and in section V conclusion is provided.

2. 2. LITERATURE SURVEY
In Deep Sub-Micron (DSM) technology, more number of gates is to be integrated on a single chip, so as to result in small geometries. Design of low power circuits are important in variety of application. Reducing power consumption involves a trade off between timing and area at different stages of the design. The successful power sensitive design requires engineers to accurately and efficiently be able to perform these tradeoffs. To handle these issues efficiently, it is essential to understand the different types and sources which play role in power dissipation in nanoscale digital circuits.

Agarwal et.al, 2006, All internal signals are set to logic values to achieve minimum total leakage current in the circuit. Since the leakage current in a CMOS gate is mainly dependent on the combinations of logic values applied to input signals. Hence such method mitigates the power consumption in CMOS semiconductor device. In another method, to increase the controllability of internal signal and to decrease the leakage current through the CMOS gates, the pMOS and nMOS transistors are added to few gates in the circuit using stacking mechanism. An experimental result of such methods on combinational circuits reduces 25% of leakage current and 5% of propagation delay.

Warren Shum and Jason H. Anderson, **2011**, presented an analysis of glitch power in FPGAs and a method for glitch reduction using don't-cares in logic synthesis. A novel

glitch reduction technique was presented that sets don't-cares in FPGA configuration bits in order to avoid glitch transitions. This method is performed after placement and routing, and has no effect on circuit area or performance.

***Jing Yang and Yong-Bin Kim,* 2013**, describes two runtime methods in their research paper to reduce leakage current in CMOS circuits. In both methods it is assumed that the device will produce a 'sleep signal' to indicate the circuit is in standby mode. In first method, pre-selected internal signals and a new set of external inputs are shifted by 'sleep' signal into the circuits.

***Zia Abbas and Mauro Olivieri,* 2014,** this paper presented a detailed study of leakage current mechanisms in CMOS image sensors. They investigated reverse current–voltage characteristics of sensors at 45 nm CMOS technology. They conclude that in p-n junction of MOS transistor, tunneling and ionization impact are the dominant mechanisms for leakage current. Similarly thermal Shockley–Read–Hall generation is the main leakage source for n-well/p-well of transistor.

***Vijay Kumar Sharma, and Manisha Pattanaika,* 2015**, The CPL (Complementary Pass Transistor) technique which generate complemented outputs in same design like AND/NAND, OR/NOR and XOR/XNOR together. This is one form of pass transistor logic only. The main drawback of the circuit is the degradation of output voltage levels due to the inability of PMOS and NMOS transistors to pass 0 and 1 respectively. The weak '0' and '1' at the sum and carry out put respectively lead to poor driving capability.

2.1 Dynamic (Switching) Power Dissipation

According to the formula:

$$P_{dyn} = V_{dd}^2 . f_{clk} . \sum_n \alpha_n . c_n + V_{dd.} \sum_n i_{sc_n} \quad (2.1)$$

the dynamic power dissipation of a digital CMOS circuit depends on the supply voltage V_{dd} , the clock frequency f_{clk} , the node switching activities α_n , the node capacitances c_n, the node short-circuit currents i_{scn} , and the number of nodes n. A reduction of each of these parameters results in a reduction of dissipated power. However, clock frequency reduction is only feasible at the architecture level, whereas at the circuit level frequency f_{clk} is usually regarded as constant in order to fulfill some given throughput requirement. All the other parameters are influenced to some degree by the logic style applied [10]. Thus, some general logic style requirements for low-power circuit implementation can be stated at this point.

2.2 Short Circuit Power Dissipation

Short-circuit currents (also called dynamic leakage currents or overlap currents) may vary by a considerable amount between different logic styles. They also strongly depend on input signal slopes (i.e., steep and balanced signal slopes are better) and thus on transistor sizing. Their contribution to the overall power consumption is rather limited but still not negligible (10–30%), except for very low voltages $V_{dd} \leq V_{tn} + |V_{tp}|$, where the short-circuit currents disappear. A low-power logic style should have minimal short-circuit currents and of course, no static currents besides the inherent CMOS leakage currents [13].

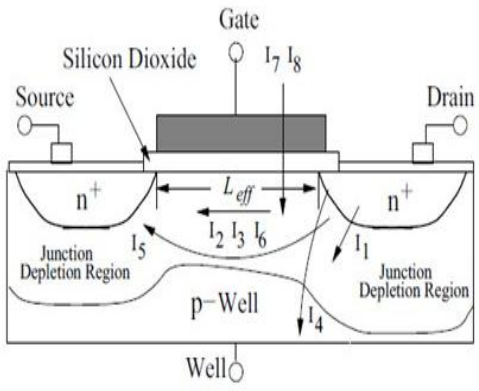


Fig.1: Leakage Mechanism In Short-Channel NMOS Transistor

Components of static power dissipation are junction leakage, sub-threshold leakage, gate-oxide leakage, gate induced drain leakage, punch through leakage and hot carrier injection. Junction leakage is due to the small reverse bias leakage current flowing between the source/drain and substrate regions. The dynamic power ($P_{dynamic}$) occurs due to the change in logic state results charging and discharging of output load capacitance. The short circuit power ($P_{short-circuit}$) dissipates when both pMOS and nMOS transistors of CMOS circuits partially ON (short- circuited) for very short duration during switching [12-14]. At the circuit level, large differences are primarily observed between static and dynamic logic styles.

Now a days the given leakage parameters are becoming the most dominating part of the total power consumption of CMOS IC. In our literature survey, different abstraction levels for power optimization of CMOS circuits are studied. Also the three main components which are responsible for power dissipation are studied and the different techniques/approaches used to minimize these components in different research papers are reviewed. In this research we also reviewed the different transistor level techniques used to design low power CMOS digital circuits. Standby mode current becomes a significant portion of the total IC power consumption, it is one of the challenge for the designers and a critical factor in low-power circuits [15].

3. PROPOSED WORK

In our work, a novel structure is proposed for low-leakage-power dissipation circuit design, in this design, we used stacking technique with pass transistor logic. Proposed circuit is compared with all other existing circuit level techniques by incorporating in conventional Gates for minimization of leakage power in nanoscale circuit designs. Proposed circuit is implemented by using two well known technique stack approach with pass transistor approach for mitigation of leakage power consumption in the existing design. Here NMOS pass transistor is connected between pull up network and pull down network which is a self controlling transistor similarly PMOS transistor is also connected between pull up network and pull down network, both the transistor are parallel to each other, both NMOS and PMOS pass transistor are self controlling transistor whch reduces the power consumption in active and ideal mode . The Pull up transistor turns ON NMOS pass transistor and Pull down transistor turns ON PMOS pass transistor during active mode of the circuit, during sleep mode both the pass transistor turns off and rail the network from the supply voltage which help in reduction of the

leakage power. Similar action also repeats in pull down network while interchanging the pass transistor NMOS transistor provide the stacking effect (Fig3.5). To maintain the value "0" in sleep mode operation, PMOS pass transistor connect parallel with NMOS transistor. To maintain an output value to "0" PMOS transistor connected to GND in sleep mode. To achieve proper logic at the output NMOS transistor is connect to Vdd and PMOS transistor is connect to GND. The stacking of the transistor reduces the leakage power in proposed approach. To maintain the proper high logic insert NMOS transistor parallel to PMOS stacked transistor in pull up network, to connect sleep transistor to Vdd to the pull up network. When circuit is in sleep mode approach, then NMOS transistor which is connects to supply voltage turns OFF and rail the circuit from Vdd for reduction of leakage power.

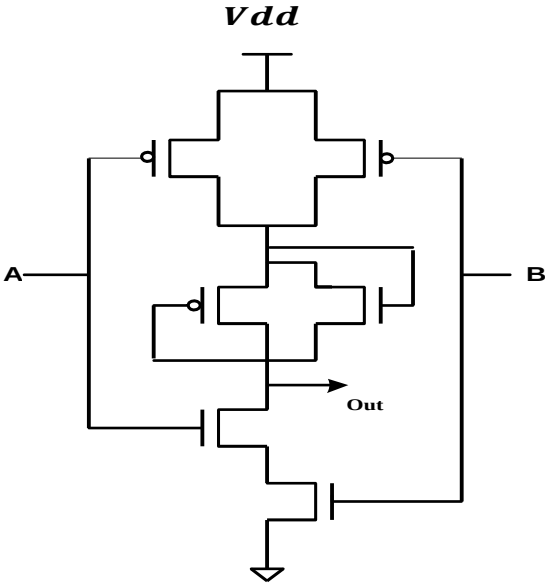


Fig. 2: Proposed Circuit

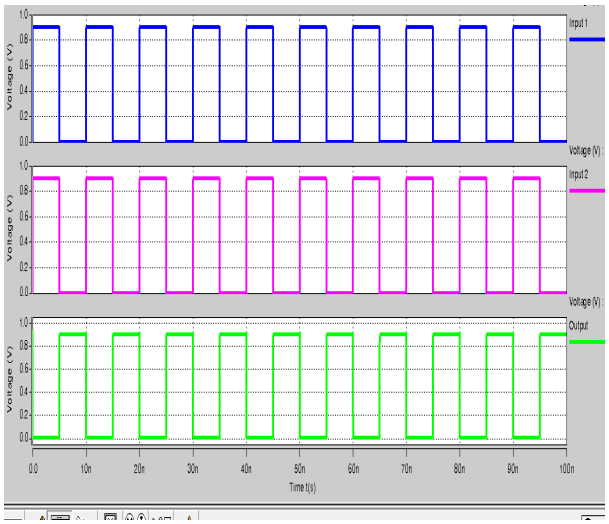


Fig.3: Output Wave form Of Proposed Circuit At 45nm

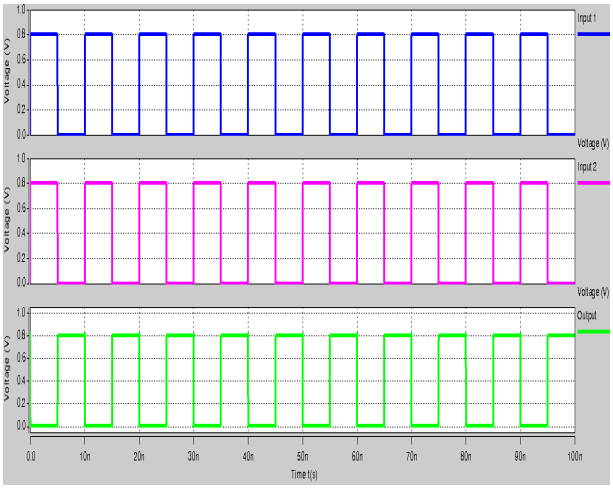
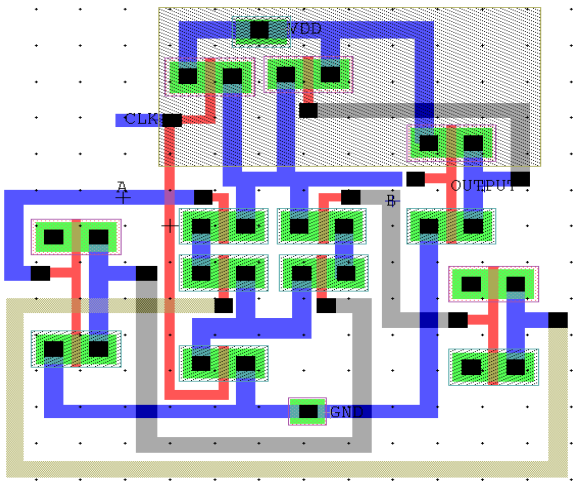
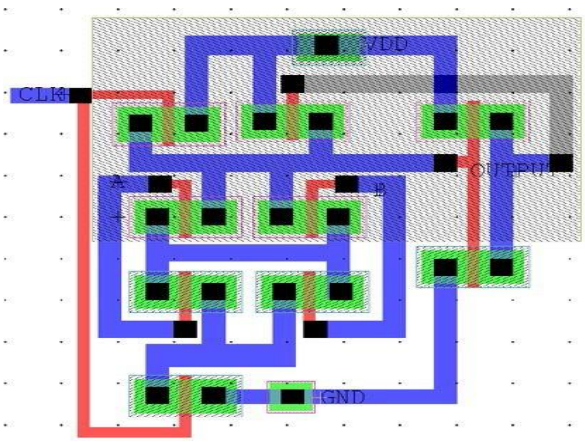


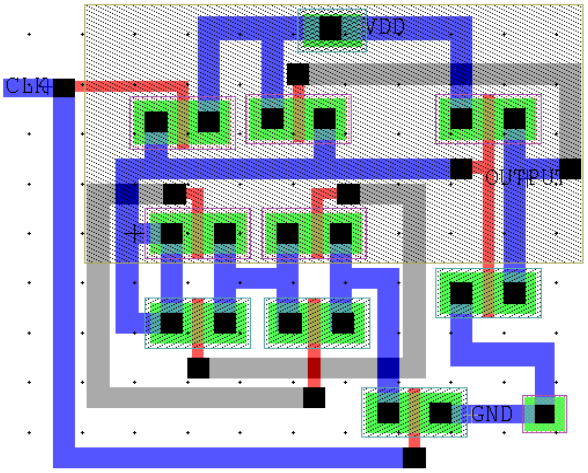
Fig.4: Output Wave form Of Proposed Circuit At 32nm



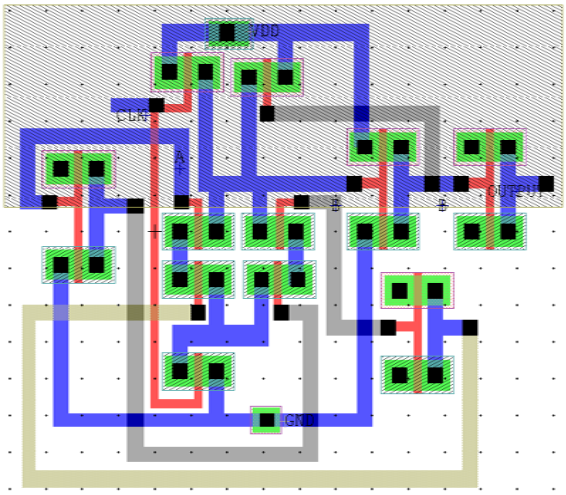
(a). Standard N-type NAND Circuit.



(b). Proposed NAND Circuit.



(a) Standard XOR circuit.



(b) Proposed XOR cicuit.

Fig. 5: Layout of Standard Proposed Circuits.

4. RESULTS AND DISCUSSION

All the simulations are performed by using SPICE simulator by using spice code (Transistor level net-list) of the desired circuit for their parameters calculation. All the circuits are mapped with 45nm and 32nm technology by using BPTM technology file. This file contains every physical design details of a CMOS transistor, where 45nm and 32nm is the effective length of CMOS transistor. Every logic circuit is implemented by two input NAND logic gate for easily understanding the approach and comparison with existing technique. DC analysis has been done for calculating I_{Leak}. For this purpose 45nm 32nm technology by using BPTM file is used at 1V and 0.9V and temperature sets at 25°C. Width to Length (W/L) ratio for the PMOS and NMOS transistors is '3' and '1.5' respectively. For DSM circuits mainly I_{SUB} is the dominating component of power dissipation in CMOS IC.

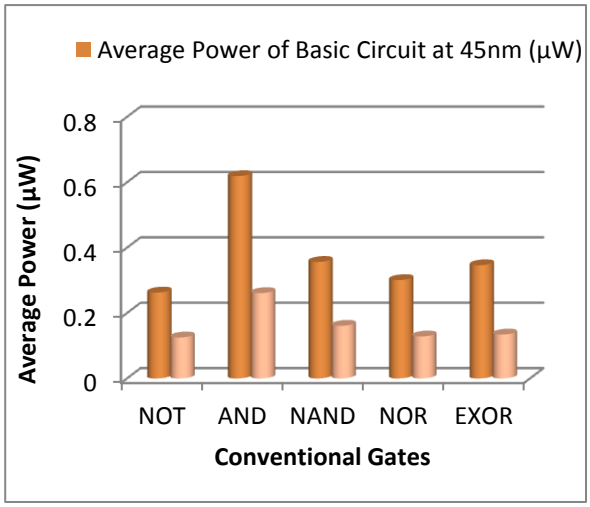


Fig.6: Dynamic power consumption at 45nm 25^{0}C

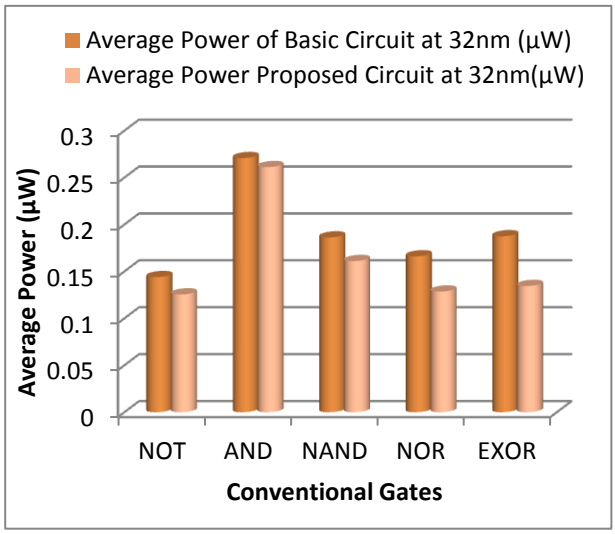


Fig.7: Dynamic power consumption at 32nm 25^{0}C

It has been clearly seen from Fig. 8 and Fig. 9, results are derived at 45nm technology at 25^{0}C temperature. These results shows comparison between basic gate design and proposed hybrid gate approach. It has been clearly shown in the bar graph, the leakage power consumption is more in basic design circuit as compared to our proposed hybrid gate technique for NOT,AND,NAND,NOR gates.

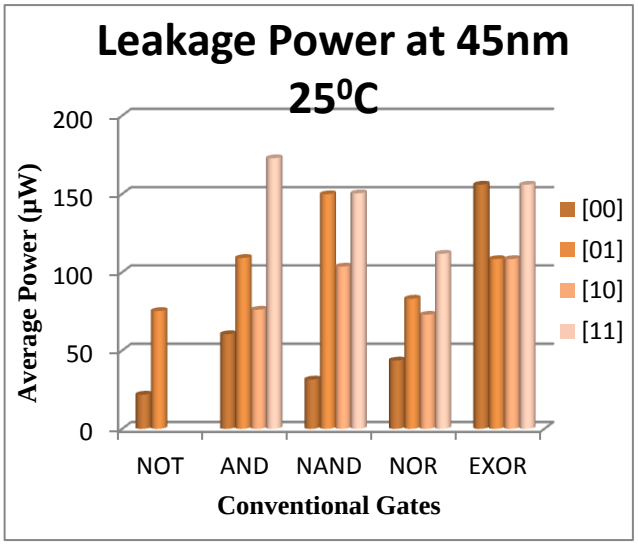


Fig.8: Leakage power for various basic gates at 45nm at 25^{0}C.

Here two input vector combination for only NOT gate i.e. 00, 01. And for all remaining gates, we applied four input vector combinations i.e. 00,01,10,11. All bar graph represents leakage power in nano-watt (nW) and four input vector combinations represented by four bar graph for each standard gate.

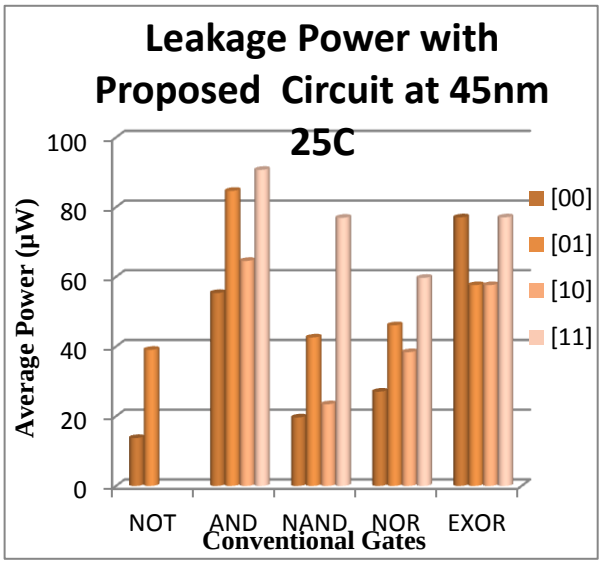


Fig.9: Leakage power for proposed various gate at 45nm at 25^{0}C.

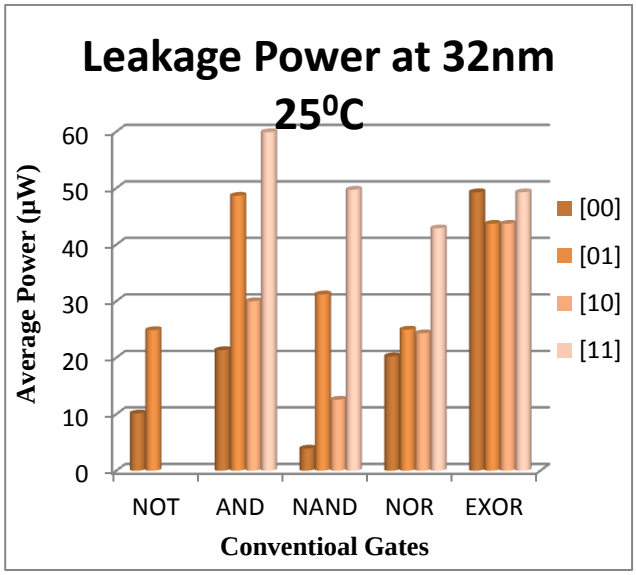


Fig.10: Leakage power for various basic gates at 32nm at 25^{0}C.

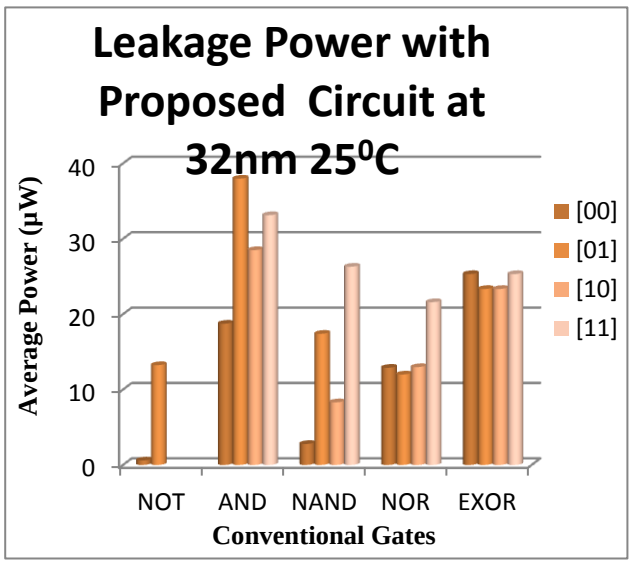


Fig.11: Leakage power for proposed various gate at 32nm at 25^{0}C

5. CONCLUSION

The research provides intense focus on leakage current/power analysis and next generation DSM technology. It reflects upon dominating face of leakage power dissipation such as I_{SUB}, I_{GATE}, and I_{BTBT} which are creating higher leakage in DSM VLSI design during idle mode. It proposes a technique for reducing the leakage current during idle mode of circuit. WLS Free Node algorithm uses four variants to effectively control I_{SUB} current of the device. This proposed algorithm gives better leakage reduction solution as compared with the other conventional and relevant techniques and there is no need of technology modification, no change of fan-out logic state of WLS gates during idle mode and needs no additional power supply. Trade–off between area, delay and power requirements can be obtained by the use of specific variant in a given circuit.

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