SoC Memory Management for Reducing Fault Problem from Reserved Memory Components

Abhijit Pathak
Lecturer
Department of Computer Science and Engineering
BGC Trust University Bangladesh

ABSTRACT
In this paper, the author proposes an optimal management for system on chip (SoC) memory by using the reserved memory components and solving the covering fault problem. This method will enable to realize many services, such as SoC diagnosis with given resolution of fault location, real-time functional testing of input patterns and analysis of output reactions.

General Terms
SoC Memory Management

Keywords
Diagnosis, system on chip, infrastructure intellectual property, fault, built in repair analysis, built in self repair.

1. INTRODUCTION
In memory management, the memory diagnosis and repair problem [1-16] is related to the tendency of continuous reduction of chip area, which is allocated to original and standardized logic, and simultaneous growth of embedded memory. At present, most of publications, which cover SoC (system on chip) testing, diagnosis and repair problems, are related to the duplication of logic elements or chip regions to double hardware realization of functionality and application of genetic algorithms for memory diagnosis and repair.

The complexity of computational hardware for modern digital systems on a chip is characterized by millions of equivalent gates and it requires developing and implementation of new high-level design technologies, such as: Electronic System Level (ESL) Design, Transaction Level Modeling (TLM) and embedded service – Infrastructure Intellectual Property (I-IP). This means that the search for high-performance methods and facilities [1] reduces all researchers to the necessity of increasing an abstraction level for the Functional Intellectual Property (F-IP) models, which are created and embedded into a chip.

There are three procedures carried out in the process of operation and repair for any type of memory:

(1) Memory testing that consists of test patterns input, which oriented on identification of specific kinds of faults [2];

(2) In the case of fault appearance, it is necessary an additional diagnosis procedure that enables to determine location, cause and kind of fault;

(3) After fault detection, which blocks carrying out of the memory function, it is necessary to activate the repair process – replacement of faulty elements by spares, which initially are on a chip [3, 4].

So, it is necessary to apply a special mechanism for memory repair, by the means of replacement of faulty components by faultless ones from the chip reserve. As a rule, the testing procedure is realized by BIST (Built-In Self-Test) block, which is hardware fast-acting generator of test patterns, as well as an analyzer (signature) of reactions of memory outputs on test patterns. (Fig. 1).

The following proposed method will enable to carry out the memory repair automatically in the operating process through embedded hardware or software implementation – a service I-IP module for fault repairing. The management of SoC memory will provide not only fast response of carrying out of functions, but also flexibility that is appropriate to software concerning design error correction.

The paper is organized as follows: Section 2 contains management SoC memory.

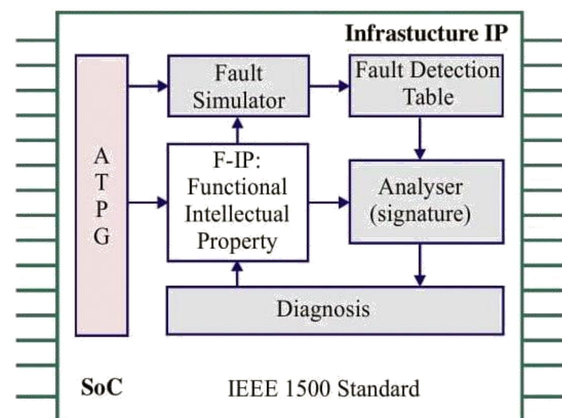

Fig. 1: Infrastructure intellectual property of SoC

Section 3 describes our proposed algorithm for management SoC memory. Section 4 includes on chip-benefits and services of the proposed method. Conclusions are given in the last section.

2. MANAGEMENT SOC MEMORY
The management of SoC memory is the representation of an exact method of memory elements diagnosis and repair by using the spares that enable to cover a set of faulty cells by the minimum possible quantity of spares. This method is oriented on implementation of the Infrastructure Intellectual Property for SoC functionality.

In fact, memory module has two parts:

(1) Functional cells, which are used for data and program storage, when a module is used in SoC;

(2) Reserve or spare cells, which are designed for memory repair in case of functional cells failure.

Functional and reserve cells are joined together in the form of columns and rows.

The repair analysis consists of definition of covering possibility of faulty memory elements by available reserve components. When a fault is detected, a row (a column), which includes a faulty element, is disconnected from the functional structure of memory cells and a row (a column) from chip reserve is connected on its place. The number of reserve components is limited, so it is necessary to apply a special mechanism of effective allocation of repair resource, for support of faulty memory elements covering by the minimum possible quantity of redundant rows and columns.

The search procedure of faulty cells covering by the minimum quantity of reserve rows and columns described above can be realized as on-chip repair module or external one [5]. In the second case data about errors is received from external modules; they are processed and pass to the controller that provides memory repair. It results in considerable time loss. So, the preferable solution is on-chip module realization, when data about errors is passed from BIST directly. Such mechanism is called as BIRA [6-8] – Built-In Repair Analysis.

Memory repair is realized by disconnection of faulty elements (rows and columns of a matrix) by means of electrical fusion of metal links and connection of reserve ones. The fuse process can be electrical or laser. Electrical fuse equipment has smaller dimensions than laser one and it is used more frequently. Fuse is carried out by means of an instruction set, which can be stored in permanent memory inside chip (hard repair) or in random-access memory (soft repair) [9, 10]. Soft repair has several advantages: when a defect appears, a new corrected instruction can be recorded to memory easily; there provide economic use of chip area and sufficient reliability. Hard repair enables to use a simplified manufacturing test and provides detection of errors, which cannot be fixed by soft repair under certain circumstances (for instance, overheat) [11].

The structure of on-chip memory analysis built-in and soft repair processes (BISR) is represented in Fig. 2.

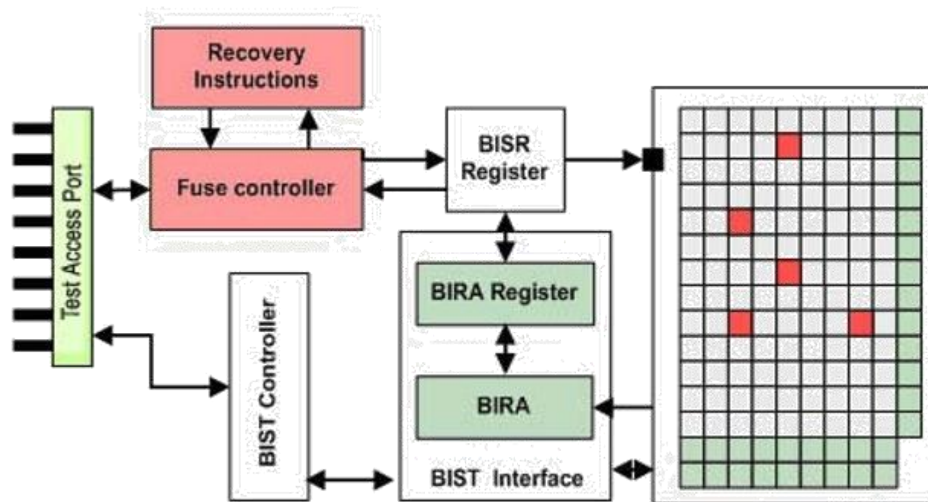

Fig. 2: Flow of on-chip memory analysis and repair

3. ALGORITHM FOR MANAGEMENT SOC MEMORY

The management algorithm steps can be summarized as follows:

(1) Chip activation, filling of the BISR register by zero values;

(2) Run the BIST controller. Memory testing and accumulation of information about faulty cells in the BIRA register;

(3) Transfer of information about faulty cells to the BISR register for subsequent fusion;

(4) Scanning the BIRA registers, which contain the repair status, by the BIST controller for obtainment of faults information;

(5) Run the fuse controller in record mode and transfer the repair instructions from the BISR;

(6) Chip restart. Recording the fuse information to the BISR register, replacement of faulty rows and columns by reserve components is fulfilled;

(7) Run the BIST controller for repeated memory testing and verification of the repair result correctness.

4. ON CHIP: BENEFITS AND SERVICES

By applying the proposed algorithm, we can obtain many benefits, services on chip, such as:

(1) Observation for state of input and output lines in functioning, verification and testing of standard blocks on the basis of utilization of the boundary scan standard IEEE 1500 [12-16];

(2) Testing of functional modules by means of input of the fault detection patterns from different test generators, which are oriented on the verification of faults or fault-free state;

(3) Fault diagnosis by means of analysis of an information obtained on the testing stage and utilization of special methods of embedded fault search on the basis of the standard IEEE 1500;

(4) Repairing of functional modules and memory after fixation of negative testing result, fault location and its type on diagnosis stage;

(5) Measurement of the general characteristics and parameters of a device operation on the basis of on-chip facilities, which enable to make time and volt-ampere measurements;

(6) Reliability and fault tolerance of a device operation in working that is obtained by diversification of functional blocks, redundancy of them and repair of SoC in real time;

(7) Finally, the practical importance of the research consists of implementation of the method to SoC Functional Intellectual Property Infrastructure.

5. CONCLUSION

In the future, system on chip memory will occupy more than 90% of chip area that is oriented on the use of flexible software.

On-chip repair is oriented on all objects, which have an address: memory, multiplexers, and matrix processors. If it is necessary to repair other structures, they must be designed with an allowance for component addressability. The addressability and regularity of components turn a system into reliable, robust, repairable and durable ones.

6. REFERENCES

[1] J. Bergeron, Writing Test Benches: Functional Verification of HDL Models, Springer, 2003, p. 512.

[2] Y. Zorian, Today's SoC test challenges, in: ITC International Test Conference, 2005.

[3] S. Shoukourian, V. Vardanian, Y. Zorian, SoC Yield Optimization via an Embedded-memory Test and Repair Infrastructure, IEEE Design and Test of Computers (2004) 200-207.

[4] V. Hahanov, W. Gharibi, K. Mostovaya, Embedded method of SoC memory repairing, Electronics and Electrical Engineering 90 (2009).

[5] P. Rashinkar, P. Paterson, L. Singh, System-on-chip Verification: Methodology and Techniques, Kluwer Academic Publishers, 2002, p. 393.

[6] Y. Zorian, S. Shoukourian, Embedded-memory test and repair: infrastructure IP for SoC yield, IEEE Design and Test of Computers (2003) 58-66.

[7] Y. Zorian, A. Yessayan, IEEE 1500 utilization in SoC design and test, in: ITC International Test Conference, 2005.

[8] IEEE-1800 IEEE Standard for System Verilog Language, 2005, p. 586, available online at: http://ieeexplore.ieee.org/servlet/opac?punumber=10437.

[9] L. Youngs, S. Paramanandam, Mapping and repairing embedded-memory defects, IEEE Design and Test of Computers (1997) 18-24.

[10] A.N. Parfentiy, V.I. Hahanov, E.I. Litvinova, SOC Infrastructure intellectual property models, ASU and Automation Devices C (2007) 83-99.

[11] V.I. Hahanov, I.V. Hahanova, VHDL + Verilog = synthesis for minutes, SMIT, Kharkov, 2007, p. 264.

[12] Z. Yervant, What is infrastructure IP, IEEE Design & Test of Computers, May-June, 2002, pp. 5-7.

[13] IEEE 1500 Web Site, available online at: http://grouper.ieee.org/groups/1500/.

[14] M. F. Bondarenko, G.F. Krivoula, V.G. Ryabtsev, S.A. Fradkov, V.I. Hahanov, Design and Diagnosis of Computer Systems and Networks, NMTS VO, Kiev, 2000, p. 306.

[15] V. Hahanov, E. Litvinova, V. Obrizan, W. Gharibi, Embedded method of SoC diagnosis, Electronics and Electrical Engineering 88 (2008).

[16] V. Hahanov, W. Gharibi, K. Mostovaya, embedded method of SoC memory repairing, Electronics and Electrical Engineering 90 (2009).