A Novel robust Design of Toffoli gate in Quantum-Dot Cellular Automata

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ABSTRACT
New practical researches on ultra-low power systems with no-loss of information for preventing heat generation as reversible gates is making many progresses in a combination with nano-scale quantum-dot cellular automata technology. In this paper, two important design factors of QCA is investigated, Then a novel robust design of Toffoli reversible gate is proposed and compared its useful template for further uses in VLSI circuits to the others.

Keywords
Toffoli , reversible gate , QCA , Boundary input , Boundary output

1. INTRODUCTION
FET-based Devices since the 1970s has been created and nowadays FETs have an incredible improvement however, FETs got serious effects making any progress in scaling more difficult because of 0.1 µm limitations at gate lengths. Feature size reduction solutions have more advantage than fighting against those effects. [1] From one side, mechanical based quantum devices keep promise of faster speeds and astonishingly reduced feature size [2] and from another side cellular automata offer many advantages like scalability, simplicity in implementation , computationally and inherently parallel.[3]

Hence, one of the most common alternative is Quantum Cellular Automata introduced in [4]. QCA is new paradigm for computing and using CA architecture in which each cell consists of a central quantum dot and four neighboring dots occupied by two electrons. Potent polarized ground states have been generated by the combination of the Coulomb Repulsion between two electrons and discrete electronic charge. QCA approach permits ultra-fast operations eliminating problems of interconnect delays, having resistive and capacitive effects, resulting ultra-low power dissipation, and making limited densities associated with conventional architectures.

In most regular ways of fabrication, QCA devices have been operated at low temperatures. Bellow a critical temperature there are no errors at all. Above that specific temperature, accumulating errors inevitably occur and make the results wrong.[4] Besides, Landauer principles are demonstrated in [5] that the erasure of one bit of information in computing process dissipates at least kTln2 Joules. As stated in [6], the computing machines which perform logical functions with no single-valued inverse, require a minimal heat generation, per machine cycle, typically of the order of kT for each irreversible function. Where k is Boltzmann's constant and T is the temperature.

Apparently, A feasible solution is reversible computing at logic level by establishing a one-to-one onto mapping between the input and output states of a circuit. As a result, dissipation can be avoided if computation is carried out with no loss of information.[7]

In this paper a novel robust design of Toffoli gate in QCA proposed which is useful in VLSI circuit designs.

The paper is organized as follows: In Section 2, Primary background information on QCA and simple basic designs discussed, then Reversible Gate Scheme is presented. In Sections 3, some related works on Reversible QCA Circuits like Fredkin and Toffoli gates are introduced, In Section 4 The proposed robust Toffoli is proposed and two practical issues are investigated and finally in Section 5, simulation results are demonstrated.

2. BACKGROUND
2.1.QCA Basics
A QCA cell consists of four quantum dots shaped in a square and two excess electrons that can occupy those dots with mutual electrostatic repulsion by each other. The cell shown in figure1A has two stable states when the cell is charged with two excess electrons. These two diagonal states represent logic 0 and logic 1 (figure 1B). The primary device to design any logic circuits such as [8] in QCA is majority gate that includes five standard cells: 3 input cells, 1 voter cell and 1 output cell. The Majority gate (figure 1C) can be operated as an OR gate or an AND gate by getting a constant input to one of the inputs. If the constant value is 0, the AND operation is performed for two other inputs. And if that is 1, the OR operation is expected from two other inputs. It can be demonstrated that NOT gate as shown in figure 1D can be simply designed.[9]

Furthermore, in [10] it has been reported a QCA design optimization methodology based on majority gates which must be directly implemented on fundamental gate instead of optimizing the design for AND–OR gates. The Designs can be illustrated in one or multi-layer such as reported in [11].

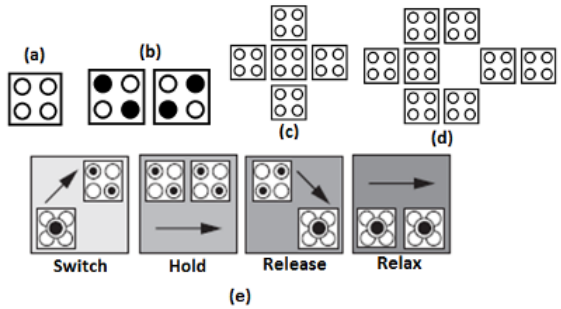

Figure 1: (a) One QCA Cell (b) Two States of Logics respectively from left to right : 0 , 1 (c) A Majority QCA design (d) a Robust NOT QCA Design (e) Four Phases Clocking scheme

QCA circuits design is partitioned into four adjacent clocking zones along one dimension known as Switch, Hold, Release and Relax. As demonstrated in figure 1E, During the Switch phase, polarization under trace of neighboring cells takes place and represents a binary logic value, electrons because of middle barriers do not switch and retain their polarity in the Hold phase. In the Release phase middle barriers are reduced and the polarity lose. In the Relax phase, there is no middle barrier and a cell do not influence on its neighbors. [12]

2.1. Reversible Design

A reversible logic function is a one-to-one onto mapping between inputs and outputs, i.e. each input pattern is mapped to a unique output pattern, while each output pattern has a unique input pattern mapped to it. Hence In Reversible computing, there is no information loss. Reversible gates are capable of restoring inputs from outputs. According to these definitions, Traditional logic functions (such as AND and OR) are not reversible, because more than one input state is mapped to a common output state.

One of the most commonly-sited reversible gates is TG in [13] The Toffoli gate which is introduced by the truth table in table 1, has three inputs(x1,x2,x3) and outputs(y1,y2,y3). Two of them are control inputs which exactly copy to the outputs (y2=x2,y3=x3) and The third output logical function is :

y1 = x1(x2)' + x1(x3)' +(x1)'x2x3

Table 1 The Toffoli Truth Table

X1	X2	X3	Y1	Y2	Y3
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	0
1	1	1	0	1	1

The basic element of designing QCA circuits is Majority Gate (MV), therefore the scheme of Toffoli gate design according to its logical scheme based on the MV gate is demonstrated in figure2 .Since it had been mentioned before, AND and OR logical functions can be represented by setting a fixed value to one of three inputs of a MV gate. [14]

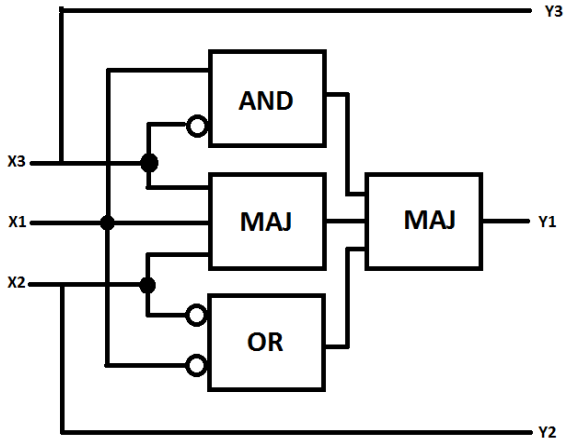

Figure 2: Toffoli Schematic reported in [14]

3. RELATED WORKS

Some useful reversible QCA gate-level designs are as follows:

3.1.Fredkin gate is introduced in [15] as a reversible logic gate and its proposed layout depicted in [14] shown in figure 3.

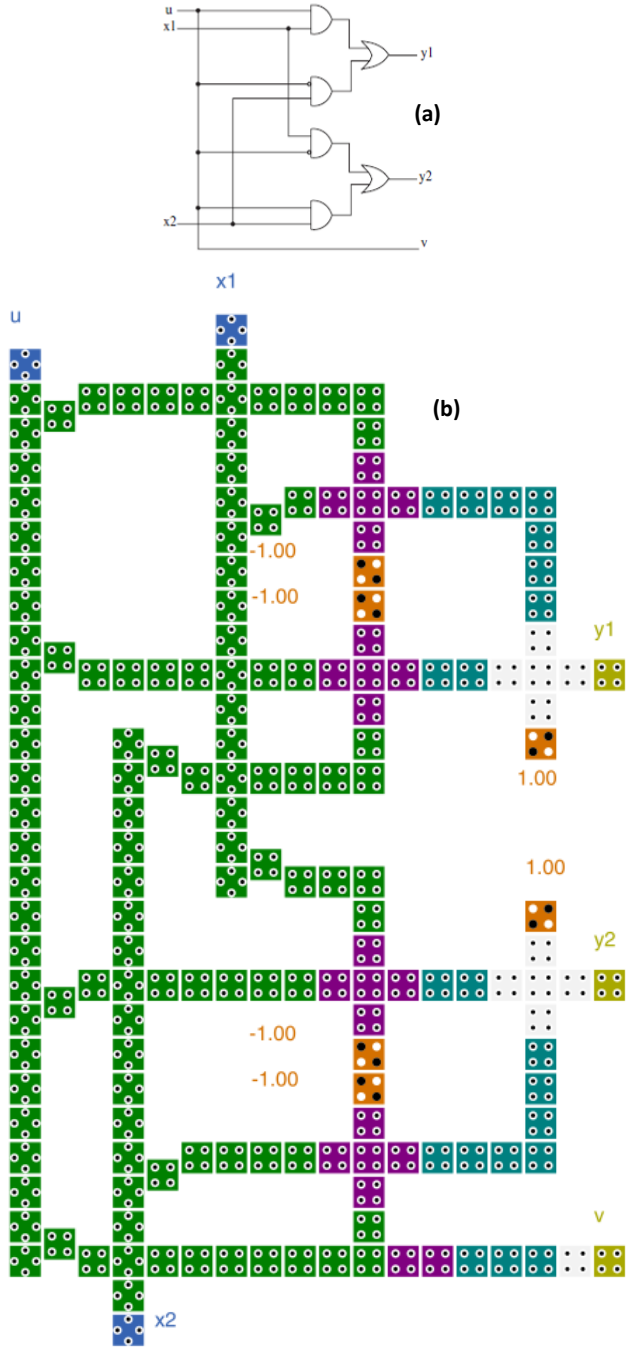

Figure 3: (a) Fredkin Schematic (b) Fredkin QCA layout in [14]

3.2.Toffoli gate is introduced in [13] and its design is reported in two ways based on their logical scheme.

1. Majority Based Designs like in [14] shown in Figure 4a which has 6 Majority gate and a new one in [16] Figure 4b.

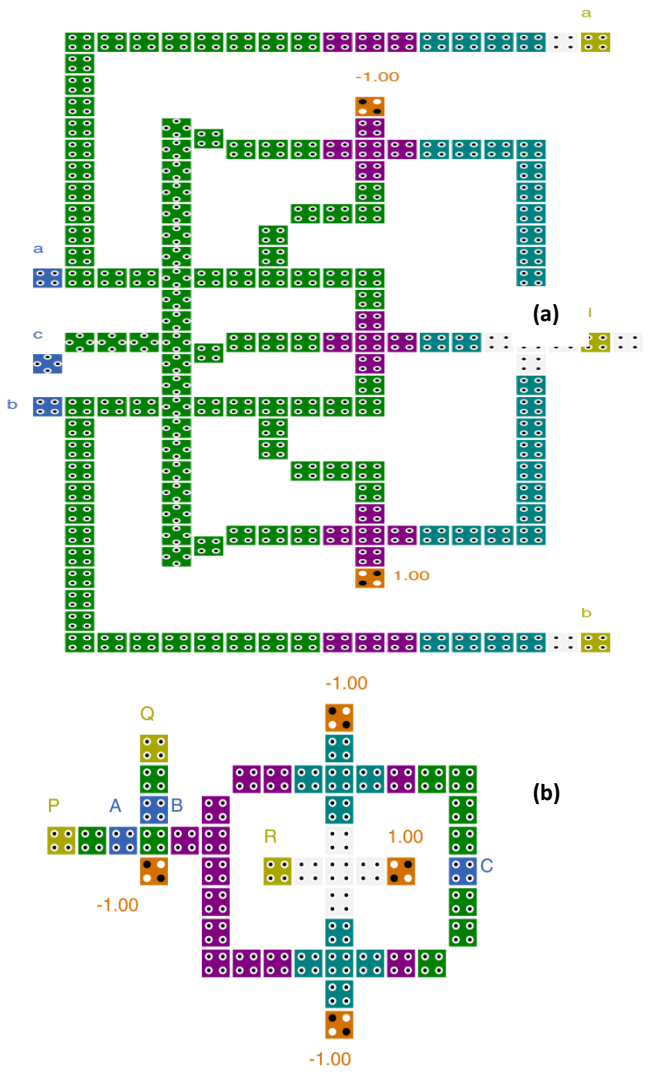

Figure 4: (a) Toffoli design reported in[14] , (b) Two Toffoli designs reported in [16]

2. XOR and Majority gate based designs like in [17] which has been mentioned in figure 5. It has just one majority and one xor gate.

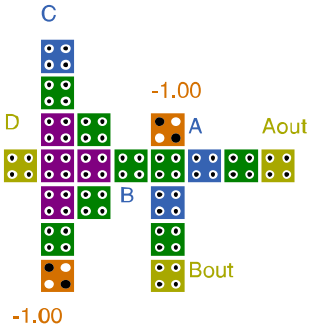

Figure 5: Toffoli design reported in [17]

4. PROPOSED DESIGN

4.1. Boundary Inputs and Outputs:

The Inputs and outputs of a QCA circuit, in order to design a VLSI extended circuit must be located in such a way that extending and deriving from them to the other blocks of design for any purpose like logic transition, can be applied without any synergic effect on the other neighbor cells and as a result without causing any change in the whole system logic. In case of non-compliance with this principle and locating the outputs in the middle of design or setting the inputs with a sticking placement closely to the majority gate, it is not possible to get any branch from them .Therefore, as one of the most effective factors of designing QCA circuits applied for VLSI designs, examining the number of these constraining inputs and outputs which called boundary inputs(BI) and boundary outputs(BO) respectively is vital. (Figure 6)

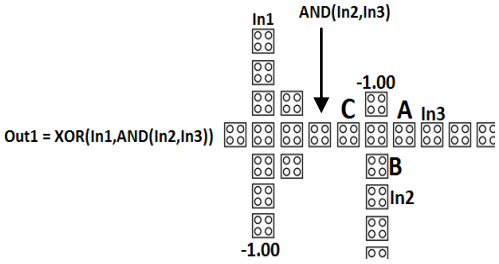

Figure 6: Proposed Toffoli Design locating Cells A,B,C

4.2.Majority Fair Voting issue

In [18] The Majority gate structure and its design rules which results properly, has been reported. Hence, Two Cells A,B in figure 4 as the proposed Toffoli gate design is placed between majority input and the input of Toffoli gate in order to reduce the number of BI and BO cells to zero. moreover, The output of the AND Block shown in figure 5 must be more amplified to be used in fairly voting in next majority block and then result properly in the next derived XOR Block. So the Cell C have to be placed after the output of the AND Block.

4.3. Proposed Toffoli Gate Design

The proposed Design is depicted in figure 7 by QCADesigner reported in [19]. Since the inputs defined in this software must be sequentially signaled, for more details, if the circuit has three inputs therefore the First input produces a signal with logical states (00001111) , the Second (00110011) and third (01010101). Therefore if there exists any changes in these sequentially assignments, the output signal will be wrong even if the design is logically depicted. The layout of the Toffoli gate designed in [17], because of the replaced inputs defined in the software and not amplifying the output signal of AND Block, has produced a signal as its output just in 3 states conforms to the toffoli truth table stated in [14]. A replacement for these two input cells makes the output signal totally conforming to its truth table.

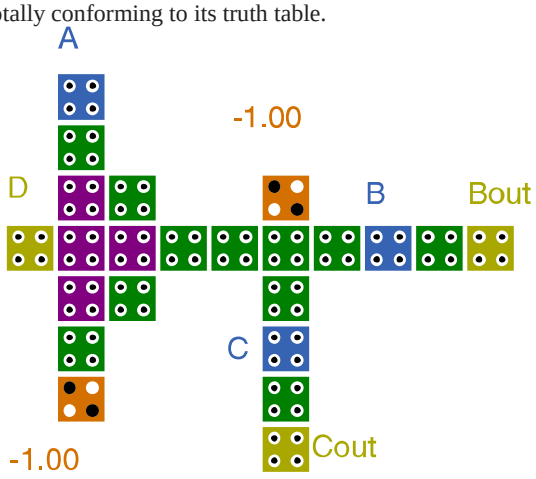

Figure 7: Proposed Toffoli Layout

Regard to the introduced layouts and importance of added factors like BIs and BOs mentioned in 3.1 and 3.2, table 2 shows a comparison between these practical issues. Though, It is clear that in the proposed design, Number of cells has been increased 3 Cells (mentioned before cells shown in figure 4 :A,B,C) and consequently the area extended from 0.034 to 0.042 , However All BIs and BOs are removed and the output signal is properly matched to its truth table. These characteristics make it optimized in VLSI circuits design. So It is demonstrated that every single design which contains BI and BO on its scheme, is not extensible.

5. CONCLUSION

In this paper, a novel robust design of a reversible quantum gate (toffoli) is proposed using quantum-dot cellular automata based on MAJ-XOR layout scheme with no boundary inputs and outputs and no unstable not, optimized for further uses in VLSI circuits, capable of deriving outputs to the other components of circuit. Future works on using this design on the other quantum gates using QCA, energy dissipation analysis of them, more MAJ-XOR layout schemes of QCA circuits are recommended.

Table 2 Comparison Table on practical issues

Design/issue	Number of Cells	Covered Area(μm^2)	Boundary Input	Boundary output	Unstable Output	Output – Truth table matching	Clocks
Toffoli [16]	48	0.0670	2 (A,B)	1 (R)	2(Nots)	100	4
Toffoli[17]	20	0.0348	2	0	1(AND)	33	2
Proposed Toffoli	23	0.0424	0	0	0	100	2

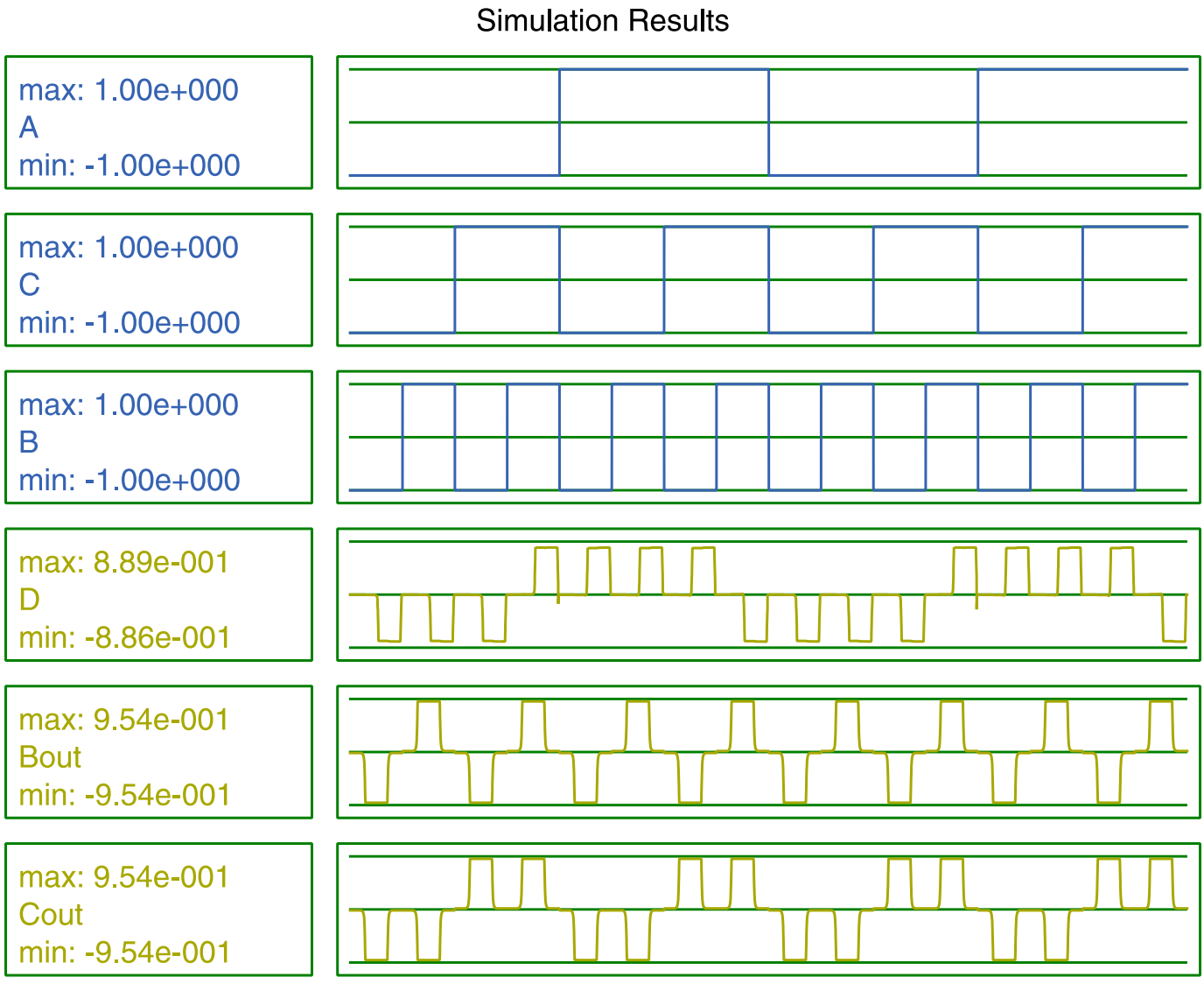

Figure 8: Simulation results: A,B,C as inputs and D,Cout,Bout as outputs

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