Abstract

Chip Interconnect delay and power is a primary criterion in the design of an Integrated Circuit because of its close connection to the speed of IC. Interconnect Buffers in VLSI circuits is the most widespread procedure used to decrease power and delay but they outcome in high Delay and power dissipation, thereby degrading the performance (i.e.) operating speed of an integrated circuit. Use of buffers within interconnect is mostly for optimizing power dissipation and delay in interconnect, but Buffers themselves possess switching time that assists to crosstalk delay and power dissipation. For effectively minimizing both delay and power dissipation in long interconnects is done via replacing buffers with Schmitt Trigger in the Nonlinear Interconnect. since Schmitt trigger have reduced threshold voltage, Schmitt trigger permits the reduction inrising time and therefore saves in periods of total delay. The proposed Schmitt trigger has a larger band gap, so it decreases the noise compare to that buffer.
Performance Optimization of Nonlinear VLSI Interconnect Circuit using Schmitt Trigger


Index Terms

Computer Science  Circuits and Systems

Keywords

VLSI, Schmitt Trigger, DSM