Performance Optimization of Nonlinear VLSI Interconnect Circuit using Schmitt Trigger

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ABSTRACT
Chip Interconnect delay and power is a primary criterion in the design of an Integrated Circuit because of its close connection to the speed of IC. Interconnect Buffers in VLSI circuits is the most widespread procedure used to decrease power and delay but they outcome in high Delay and power dissipation, thereby degrading the performance (i.e.) operating speed of an integrated circuit. Use of buffers within interconnect is mostly for optimizing power dissipation and delay in interconnect, but Buffers themselves possess switching time that assists to crosstalk delay and power dissipation. For effectively minimizing both delay and power dissipation in long interconnects is done via replacing buffers with Schmitt Trigger in the Nonlinear Interconnect. since Schmitt trigger have reduced threshold voltage, Schmitt trigger permits the reduction inrising time and therefore saves in periods of total delay. The proposed Schmitt trigger has a larger band gap, so it decreases the noise compare to that buffer.

Keywords
VLSI, Schmitt Trigger, DSM

1. INTRODUCTION
In deep submicron (DSM) technologies, interconnects none longer act as Resistors but may possess affiliated parasitic such as capacitance and inductance. With a linear improve in interconnect length, both the interconnect capacitance (C) and interconnect resistance (R) enhanced linearly, producing the RC delay increase quadratically. Even though the RC delay is not a precise approximate of the time needed for a signal to propagate through a cable, the total RC delay of a section of a line may be useful as a figure of merit. In lead to enhance the computation speed of an integrated circuit, it is required to diminish the RC delay. In supplement to enhanced signal propagation delay, increased power dissipation is another result of large interconnects impedance. Buffer insertion is evolving a bulky method for DSM technologies to diminish interconnect delay, calling for to pinpoint the solution with adifferent approach. The objective of the paper is to develop another option approach to Buffer Insertion for delay, power and noise reduction within VLSI interconnect in DSM technology.

Delay and noise are two equivalent factors in DSM technology. For signal restoration and to handle the on-chip delay and noise, buffer insertion technique has been modified, and Schmitt trigger is employed to replace it in VLSI interconnects at all the probable nodes. In Schmitt trigger, the threshold voltage of the device can be adjusted, so if it is set to reduced, then it can get an early increase in rising signals and therefore less propagation delay.

Buffer insertion procedure is to find where to add buffers in the interconnect inorder that the timing prerequisites are met. Since the propagation (Elmore) delay has a square dependence on the length of an RC interconnects line, subdividing the line into shorter sections is an effectual approach to deteriorate the total propagation delay [2].

Owing to the enormous drop in VLSI feature size, a massive figure of buffers are Needed for accomplishing timing objectives for interconnects. It is asserted in a recent study [3] that the number of nets that require buffer insertion and the number of buffers will surge dramatically as shown in Figure 1.

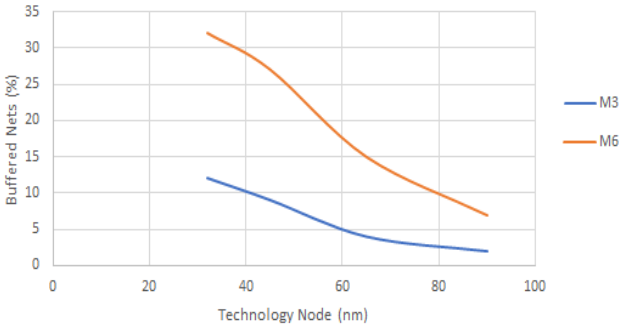

Fig 1: Percentage of Nets Requiring Buffers.

2. NEED FOR A BETTER APPROACH
Buffer Insertion is a very effective approach for delay reduction. But as is noticeable from the above section, in every new generation deep submicron technology, buffer insertion is becoming a principal complication, because of their number and also because of they now a principle cause of power dissipation. Hence a trade-off is required between delay and power consumed. Thus, there is a need for a novel strategy that while reducing the delay, also uses less power.

One of the foremost limitations of buffer inclusion is the increasing number of repeaters within the system. Figure 1 shows the increasing percentage of total buffered nets in every technology node. Similarly, Figure 1 shows the increase in a buffered cell with each next technology. Hence buffers are occupying a major portion of the total area in the system. Similarly, this clearly demonstrates the exponential rise in the area consumed by buffers for Different interconnect length.

All these factors are not in supportive for buffer insertion for interconnect modeling. Thus, a foremost discovery is required towards handle interconnects. Hence holding within the mind of all the annoyances being faced and to be originating with buffer insertion, in this paper, other option to buffer is recommended for linear Interconnects.

2.1 Schmitt Trigger

Schmitt trigger can be altered to deal with analog input signals. The principle intent of Schmitt trigger is to restore the form of digital signals. Hence this element can replace buffer as far as restoring the signal is concerned. Because of the transmission line, there is thetransformation of digital form from square to more complex signal. While transmitting signal, it may become noisy.

Schmitt trigger is a comparator with positive feedback, and furthermore possess dual threshold voltage what end in hysteresis, which means between the lower (U1) and the upper threshold (U2) of Schmitt trigger the state of output never change. This result outcome in the stabilization of output.

The main advantage of Schmitt trigger is its noise immunity due to its greater band gap and single input threshold which permits signal to switch rapidly. Schmitt Trigger can be implemented using 6 CMOS transistors. This implementation ensures more noise reduction and early rise and fall of thesignal, which determinants less propagation delay too. Thus, whether Buffer is replaced with Schmitt trigger in interconnects, it is expected to accomplish more noise, delay and power reduction.

The classic Schmitt trigger is realized employing an op-amp with two resistors to accomplish a regenerative feedback. The circuit representation of Schmitt trigger is shown in Figure 2.

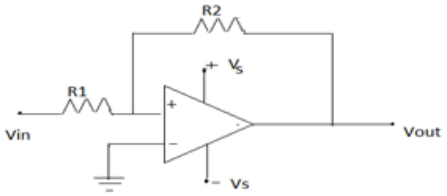

Fig 2: Schmitt Trigger Implementation with Comparator.

2.2 2.2 CMOS Schmitt Trigger

In bipolar technology, p-n-p transistors are much slower than their n-p-n equivalent and the bipolar prototype for the every component of the circuit. A bipolar Schmitt trigger encompasses an n-p-n differential pair loaded with a resistor. The circuit of Figure 3 embraces two similar subcircuits (M1, M2, M3 and M4, M5, M6). Each of them is a greatly nonlinear load for the other. However, as guided subsequently, at each transition point, one sub-circuit can be examined as a linear resistive load for the other. In the circuit of Figure 3, the bottom circuit MI, M2, M3 (which issummoned here the N-sub circuit), is stacked by the top circuit, M4, M5, M6 (P-sub circuit). As an issue of the circuit symmetry, the inverse assertion is additionally valid.

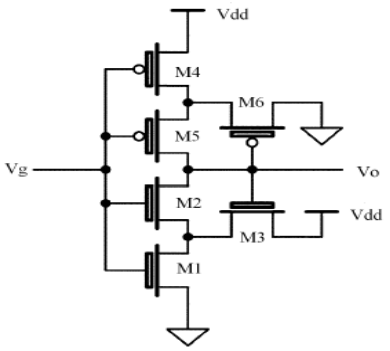

Fig 3: Low voltage CMOS Schmitt trigger.

3. SYSTEM ARCHITECTURE

Figure 4 shows the system architecture.

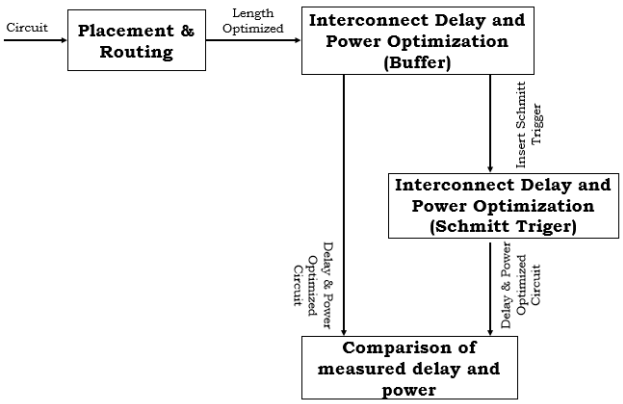

Fig 4: System Architecture.

3.1 Placement And Routing

Placement and Routing are done in alignment to reduce the interconnect length; thereby prerequisite of theplacing of some Schmitt triggers will be less, thus efficiently reduce the delay and power. The principle objective of Routing is to accomplish all circuit connections using the shortest possible wire length [4]. Native Circuit Description (NCD) file is produced after running Map program. That design file is utilized for Placement and Routing. Placement and Routing is done based on two criteria, i) Timing-Driven & ii) Non-Timing-Driven.

Timing-Driven

Placement and Routing are done grounded on Timing Constraints.

Non-Timing-Driven

Placement and Routing are done ground upon such pertinent constraints, thelength of connection, available resources but no time constraints are present.

3.2 3.2 Interconnect Delay And Power Optimization(Buffer)

Buffer insertion is one popular technique to decrease (eliminate) the delay. In this technique, buffersare placed at regular intervals along an interconnect that seeks towards reestablishing the signal each time it is influenced by the parasitics. However, buffers themselves possess certain switching time that contributes todelay. Many such buffers along an interconnect can thus contribute towards overall delay to signal propagation. Also, buffer switching contributes to power dissipation [5].

Further in DSM technologies, leakage power is a foremost difficulty and buffers may consume power even as shortly as they are not switching. Thus, there is an imperative need to evolve techniques that while reducing the overall delay, in addition, consume lesser power, dynamic as well as static. Buffers themselves possess certain switching time that assists in delaying. A wide number of such buffers along an interconnect therefore assist to overall delay to signal propagation. Also, buffer switching assists to power dissipation[6] .

Further in DSM technologies, leakage power is a major problem and buffers may consume power even when they are not switching. Thus, there is an urgent need to evolve techniques that while reducing the overall delay, also consume lesser power, dynamic as well as static [7].

The design is implemented in a VHDL IDE (for FPGA implementation such as Xilinx ISE, Altera Quartus, Synopsys Simplify or Mentor Graphics HDL Designer) to generate the RTL schematic of the desired circuit. The buffer is inserted in the interconnect and delay, and power is measured.

3.3 Interconnect Delay and Power Optimization (Schmitt Trigger)

Schmitt triggers as an alternative to buffering to decrease the power and delay, in non-linear interconnects. Most favourable characteristic of Schmitt trigger is its adjustable threshold voltage, and it can be get controlled, in order that threshold voltage can be chosen to be above or below $^{v_{dd}}/_{2}$ where buffer generally operate [8].

Schmitt trigger can switch faster than the buffer, the delay can be decreased substantially by Schmitt trigger contrast to that of buffer, and since buffer needs more power for switching and refreshing, power dissipation is less by usage of Schmitt trigger. The lower threshold of the Schmitt trigger permits the deterioration in rising time and hence saves in terms of total delay. Although the storing in rising time delay are a couple of pico-seconds only, is very significant.

With the invent of Schmitt trigger, all kinds of bus coding techniques can be neglected and therefore effecting in adecrease of additional power and hardware utilization by those transistors. The additional hardware which is needed in the configuration of encoder and decoder for bus coding techniques is also not required. Hence area savings may also be achieved. The output is delay and power optimized non-linear interconnects [9].

Schmitt trigger can behave as a signal restoring circuit, the primary cause why we have gazed into the advance of engaging Schmitt trigger as an alternative of thebuffer in interconnects acts as a data restoring element. Reduced noise glitches effects in lesser power utilization and therefore assist in decreasing the total power that gets consumed. Noise immunity of Schmitt trigger is more than buffer due to larger band gap [10]. The most favorable characteristic of Schmitt trigger is its adjustable threshold voltage, and since it can be controlled, the threshold voltage can be chosen as below or above $v_{dd} = 2$ a voltage at which buffer usually operate [11]. Thus, a Schmitt trigger can be conceived to switch much quicker than buffer that is directing to a decrease in delay. Further, the Schmitt trigger's adjustable low-voltage threshold manages more voltage and noise glitches as equated to buffer. It is shown that the proposed approach is better in terms of delay, power and crosstalk noise reduction compared to that of buffers [12].

4. RESULTS

Two different circuits were taken into consideration

1. Transmitter Circuit (Circuit 1)
2. Receiver Circuit (Circuit 2)

4.1 Delay Measurement

The delay of the Transmitter Circuit under Interconnect Buffer and Schmitt Trigger approaches is measured, and it is observed that Schmitt Trigger approach is better and the delay is 32% less than the delay of interconnect buffer method as shown in Figure 5.

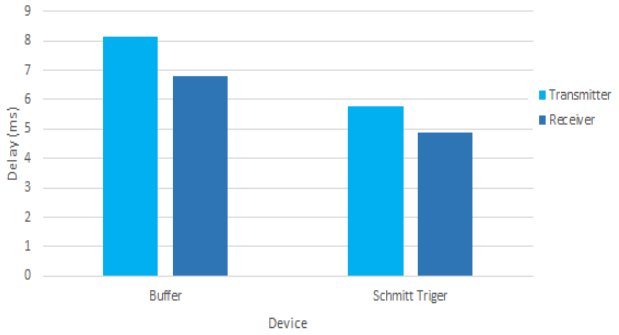

Fig 5: Delay (Transmitter & Receiver Circuit)

The delay of the Receiver Circuit under Interconnect Buffer and Schmitt Trigger approaches is measured, and it is observed that Schmitt Trigger approach is better and the delay is 30% less than the delay of interconnect buffer method Figure 5.

4.2 Power Measurement

The power of the Transmitter Circuit under Interconnect Buffer and Schmitt Trigger approaches is measured, and it is observed that Schmitt Trigger approach is better and the power consumed is 80% less than the power consumption of an interconnect buffer method Figure 6.

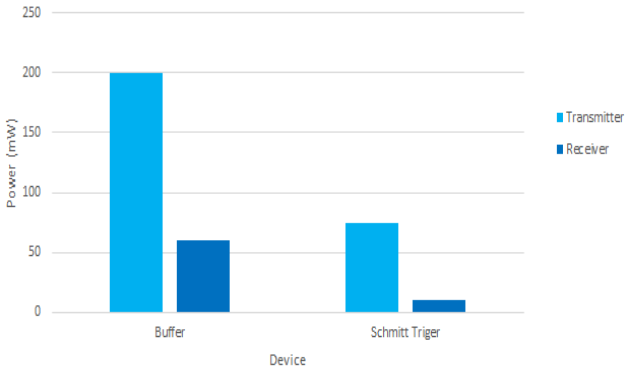

Fig 6. Power (Transmitter & Receiver Circuit).

The power of the Receiver Circuit under Interconnect Buffer and Schmitt Trigger approaches is measured, and it is observed that Schmitt Trigger approach is better and the power consumed is 83% less than the power consumption of an interconnect buffer method Figure 6.

5. CONCLUSION

Thus, Delay and Power Dissipation is less in thecase of Schmitt Trigger due to its Low Threshold Voltage, drop and rise of the signal will be afaster contrast to that of Buffer. Moreover, Schmitt Trigger does not Require Power for Refreshing. So, Interconnect Delay and Power Consumption is substantially decreased under the usage of Schmitt Trigger. In future, the same technique can be applied to Linear and Non-Linear RLC Circuits, delay and power can be assessed and weighed against to Buffer.

6. REFERENCES

[1] Sandeep Saini, A. Mahesh Kumar, Sreehari Veeramachaneni. 2010. An Alternative approach to Buffer Insertion for Delay and Power Reduction in VLSI Interconnects. 23rd International Conference on VLSI Design. pp. 411-416.

[2] Y.I. Ismail and E.G. Friedman. 1999. Effects of inductance on the propagation delay and repeater insertion in VLSI circuits. Proceedings of the Conference on Design Automation, New Orleans, Louisiana, pp. 721-724.

[3] P. Saxena and N. Menezes and P. Cocchini and D.A. Kirkpatrick. 2004. Repeater scaling and its impact on CAD". IEEE Transactions on Computer-Aided Design. 23(4), pp. 451-463.

[4] H. Zhou, D. F. Wong, I. M. Liu, and A. Aziz. 2000. Simultaneous routing and buffer insertion with restrictions on buffer locations. IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems. 19(7), pp. 819-824.

[5] C. C. N. Chu and D. F. Wong. 1999. A quadratic programming approach to simultaneous buffer insertion/sizing and wire sizing. IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems. 18(6), pp. 787-798.

[6] J. Lillis, C. K. Cheng and T.-T. Y. Lin. 1996. Optimal wire sizing and buffer insertion for low power and a generalized delay model. IEEE Trans. Solid-State Circuits. 31(3), pp. 437-447.

[7] C. J. Alpert and A. Devgan. 1996. Wire segmenting for improved buffer insertion. Proceedings of ACM/IEEE Design Automation Conference. pp. 588-593.

[8] H. B. Bakoglu and J. D. Meindl. 1985. Optimal Interconnection Circuits for VLSI. IEEE Transactions on Electron Devices. 32(5). pp. 903-909.

[9] S. Yu et al. 2006. Loop-Based Inductance Extraction and Modeling for Multiconductor On-Chip Interconnects. IEEE Transactions on Electron Devices. 53(1), pp.135-145.

[10] T. Dhaene and D. D. Zutter. 1992. Selection of Lumped Element Models for Coupled Lossy Transmission Lines. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. 11(7), pp. 805-815.

[11] M. A. El-Moursy and E. G. Friedman.2003. Optimum Wire Shaping of an RLC Interconnect. Proceedings of the IEEE Midwest Symposium on Circuits and Systems.

[12] Sherwani, N.A. 1995. Algorithms for Physical Design Automation. 2nd Edition. Kluwer Academic Publishers Norwell, MA.USA. ISBN: 0792395921.