Reconfigurable Memristor and CNFET based Four Quadrant Multiplier for Low Power Applications

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ABSTRACT
In this paper, a reconfigurable, low power four quadrant memristor and carbon nanotube field effect Transistor (CNFET) based analog multiplier is proposed. The circuit is verified by extensive HSPICE simulations using experimentally verified memristor and Stanford CNFET models that have been calibrated for 90% accuracy at the 32nm technology node. The proposed multiplier has an input range of ±0.25V, extremely large bandwidth of 30.5 GHz, and consumes just 43.8μW of power along with low total harmonic distortion (THD% ≤0.75) and significant noise suppression at a supply voltage of ±0.3V.

Keywords
CNFET; memristor (M); analog multiplier; amplitude modulation; low power.

1. INTRODUCTION
Analog multiplier is an important building block of analog signal processing systems. It is used as a sub-circuit for many applications such as adaptive filters, modulators, phase comparators, frequency mixers, and neural networks [13]. It performs linear product of two analog input signals x and y, yielding an output z=*K*xy, where '*K*' is a constant of proportionality [2]. The basic principle involved in the design of a multiplier is a quarter square algebraic [24]. There are three operations which need to be performed. The first operation to be performed is the summation and difference of the input signals. The second step is the squaring of the obtained sum and difference. In the last step, the output is taken as the difference between the obtained squared signals. Motivated by the work of Gilbert [10], multipliers have been designed and optimized for a variety of applications [11] [18][26][31]. The basic idea behind these designs is the utilization of active devices like CMOS to process/condition the input signals followed by the neutralization/minimization of errors due to the non-linear characteristics of these devices. Active devices are continuously scaled to achieve high packing density, high speed and low power consumption. Due to leakage current, high field effect, short channel effect and lithographic issues associated with CMOS. Moore's law [23] cannot hold forever and there is a need to explore emerging devices [32] [33] [34] like TFET or CNFET that has the potential to replace existing bulk CMOS along with a memristor to sustain Moore's law far in the future. This paper proposes a memristor and CNFET based multiplier that operates at low voltage with high linearity, large input signal swing and better frequency response.

The remainder of this paper is organized in the following sections. Memristor and CNFET are introduced in section 2. The proposed multiplier is illustrated in section 3. The simulated results of the proposed multiplier are then presented in Section 4 followed by conclusion in section 5.

2. EMERGING DEVICES
2.1 Carbon Nano Tube based FET (CNFET)
Device Engineers in the past have been concentrating on scaling the CMOS technology down to the nanometer range for better and superior performance. As per International Technology roadmap for semiconductor (ITRS) predictions [14], gate length of MOS devices would be less than 10nm by the end of 2015, which means that CMOS technology would face enormous challenges due to high channel doping, band tunneling across the junction and gate induced drain leakage (GIDL), high field effect, lithographic limits and quantum confinement effect. There is a need to explore newer devices beyond bulk CMOS. Carbon Nanotube Field effect Transistors (CNFETs) hold a promising future among the upcoming nano-electronic devices due to its ballistic transport capability, narrow diameter of the order of few nanometer, superior electrostatic and structural properties [6] [7]. Carbon nanotube is made by rolling up a sheet of graphite or graphene (a monolayer of sp2 bonded carbon in a honeycomb lattice) into a cylinder. It exhibits remarkable electrical properties that make atomic electromigration more difficult. This means that carbon nanotubes have a stable structure that avoids damage from high currents [22]. Carbon nanotubes(CNTs) are hollow cylinders of graphene having varying diameter (0.4nm to 4nm) and it provides a single path between source and drain. They can be classified depending upon the direction in which the graphene sheets are rolled up either as semiconducting with distinct band gap or metallic with no bandgap. The resulting structure is called single-walled carbon nanotube (SWCNT). If more than one SWCNT of varying diameters are folded concentrically, they form a multi walled CNT (MWCNT). The properties of CNTs such as bandgap, conductivity, diameter etc. are determined by its chirality (n1, n2). A SWCNT works as metal if n1 = n2 or n1 – n2 = 3i, where 'i' is an integer. Otherwise, it works as a semiconductor. The relationship between chirality (Ch), CNT diameter (D_{CNT}) and threshold voltage (V_{th}) is given by:

$$Ch = a\sqrt{(n_1^2 + n_2^2 + n_1 n_2)} \quad (1)$$

$$D_{CNT} = Ch/\pi \quad (2)$$

$$V_{th} \approx \frac{E_g}{2} = \frac{aV_\pi}{qD_{CNT}\sqrt{3}} \quad (3)$$

Where Eg is the energy gap, q = electronic charge, a = √3d = 2.49 Å is the lattice constant (where d = 1.44 Å is the inter-carbon-atom distance) and Vπ =3.033eV is the carbon π–to–π bond energy in the tight bonding model [17] [21]. The working principle of CNFET is similar to that of conventional MOSFET. The bulk semiconductor channel is replaced by a

number of semiconducting carbon nanotubes as shown in Fig. 1. Since the carriers are now confined to a narrow nanotube, their mobility increases due to quasi 1-D (ballistic) transport.

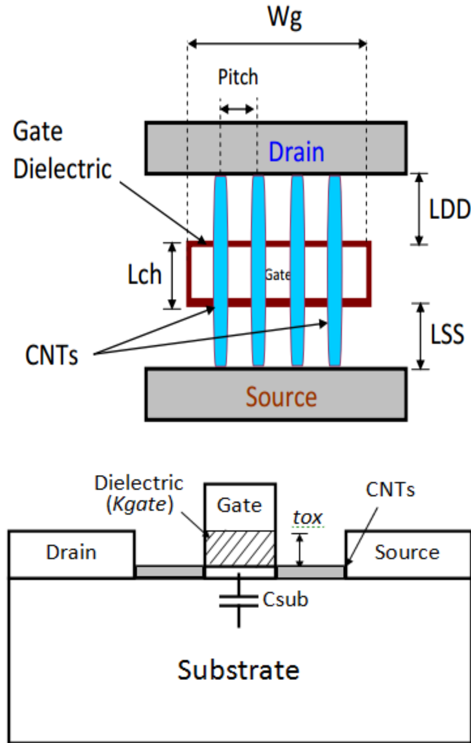

Fig.1. Carbon nanotube field effect transistor

This paper deals exclusively with SWCNTs only and the multiplier circuit is operated in the voltage range from ±0.3V to ±0.9V, therefore it has been implemented using SWCNTs due to higher drive current and transconductance, lower on resistance and negligible off current as compared to MOSFET.

2.2 Memristor

Memristor was hypothesized by L.O. Chua, [3]. The idea was based on a simple symmetry argument that a fourth fundamental 2-terminal passive circuit element is necessary to complement the other three. The memristor is like a potentiometer which permits continuous change in its resistance. It differs from potentiometer in the sense that a memristor has only two terminals and the resistance is changed by applying different writing and erasing potentials across the device. It can remember its previous state when power is removed, and hence the device has memory.

The physical device consists of a thin layer of TiO2 (Titanium dioxide) sandwiched between two metal contacts made of Pt (Platinum) as shown in Fig. 2. The oxide film is divided into two regions: a doped region of TiO_{2-x} with low resistance R_{ON} due to the high concentration of dopants and an undoped region of TiO_2 with high resistance R_{OFF}. The ratio between the two is controlled by the position of the boundary between the doped and undoped regions. As the device has extremely small dimensions, a very strong electric field develops when a voltage is applied. This causes the oxygen vacancies to move towards or away from the doped region effectively changing the position of the boundary between the two regions and hence the total resistance of the device [8].

The total resistance of the memristor, R_{mem}, can be modelled as the sum of the resistances of the doped and undoped regions.

$$R_{mem}(x) = R_{ON}x + R_{OFF}(1-x) \quad (4)$$

$$x = \frac{w}{D} \in (0,1) \quad (5)$$

R_{ON} is the resistance of completely doped memristor and R_{OFF} is the resistance of completely undoped memristor corresponding to w=D and w=0 respectively where 'w' is the width of the doped region and 'D' is the total width of the memristor.

The relation between excitation voltage and current flowing through the memristor is

$$v(t) = R_{mem}(w)i(t) \quad (6)$$

The dependence between the passing current 'i' and the *x* state is governed by the dynamic state equation [8].

$$\frac{dx}{dt} = kf(x)i(t), \qquad k = \frac{\mu_v R_{ON}}{D^2} \quad (7)$$

Where μ_v is the average dopant mobility. The function f(*x*) in equation (7) is a window function and models the non-linearity of the charge carrier transport in the memristor [15].

$$f(x) = 1-(2x-1)^{2p} \quad (8)$$

where 'p' is an integer

Apart from having nanoscale dimensions, memristor has other useful properties like reconfigurability, continuous resistance range, low-power consumption etc. There are many applications of memristors. Analog programmable circuits have already been explored theoretically, mostly through simulations. Some of the examples are: Analog filters, gain amplifiers, threshold comparators, switching thresholds Schmitt triggers and frequency relaxation oscillators [9] [25] [28] [29]. In all these examples, characteristics of the circuit were configured by adjusting the resistance of the memristor.

3. PROPOSED MULTIPLIER

The idea behind the design of proposed multiplier is the quarter square algebraic identity [24]. The proposed multiplier circuit is shown in Fig. 3. It consists of two stages. The first stage is the adder subtractor stage consisting of memristive voltage dividers and the second stage is the multiplier core where input voltage is first converted to current and finally current is converted to voltage and differential output is taken. The differential output can be expressed as:

$$V_{out} = \left[(V1+V2)^2 - (V1-V2)^2\right] = 4V1V2 \quad (9)$$

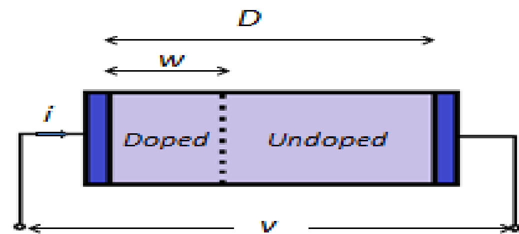

Fig.2. Basic Structure of memristor

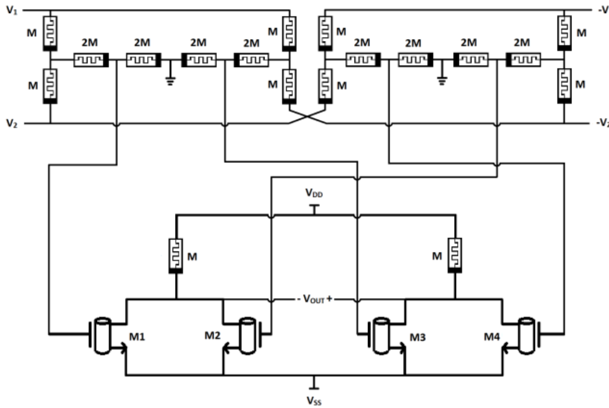

Fig.3. Proposed multiplier circuit

The most prominent feature of the proposed multiplier is its reconfigurability due to memristive voltage divider. Apart from that its area can be estimated to be smaller than other multipliers because of the nanoscale memristive devices. Also the memristive voltage divider functions as an adder and a subtractor for a large range of frequencies. All these features make this multiplier suitable for portable systems where power consumption is an important factor.

4. SIMULATION RESULTS

The proposed memristor and CNFET based multiplier circuit is designed and simulated using HSPICE simulator incorporating 32nm CNFET model and memristor model [1] at a supply voltage of ±0.3V . The performance of the multiplier such as power, linearity and bandwidth are severely affected by the diameter of the CNTs. The diameter of CNT(D_{CNT}), its bandgap energy Eg and the threshold voltage of the device (V_{th}) are related by the following equations

$$Eg = 0.84\ eV / D_{CNT} \qquad (10)$$

$$V_{th} = Eg / 2e \qquad (11)$$

Where 'e' is the electronic charge. D_{CNT} not only affects the source/drain series resistance but also the threshold voltage of CNFET. It is observed from the simulation results that with the increase in the diameter of the nanotube as shown in Fig. 4, bandwidth, and power consumption of the multiplier increase. These trends can be justified by the decrease in the gate to channel capacitance along with fringe capacitance. This decrease in capacitance is due to enhanced screening between adjacent CNTs [6] [7]. However, it is to be noted that for large values of D_{CNT}, the current saturates because of large screening and scattering effects thereby severely affecting the linearity of the circuit. The CNTs are therefore optimized for their most practical values, a compromise between circuit requirements and a trade-off is involved between the 3-dB bandwidth, power and linearity. The optimum diameter value is hence chosen to be 0.9 nm corresponding to chiral vector (11, 0). Table 1 and 2 show the optimized CNFET and memristor parameters used in the simulation of the proposed multiplier. The performance evaluation of the multiplier is carried out on the basis of key parameters namely DC transfer characteristics, harmonic distortion analysis, frequency response, low voltage operation, low power consumption and noise analysis at a supply voltage of ±0.3V corresponding to a input of 0.1V.

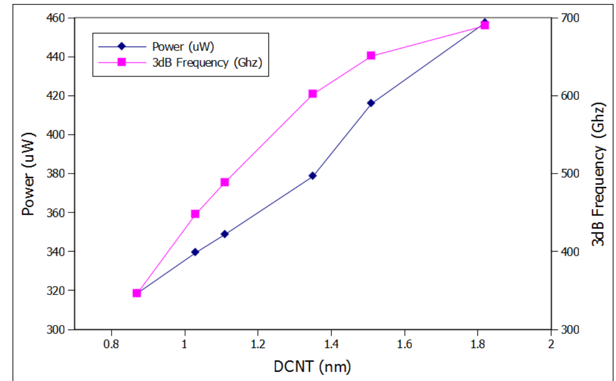

Fig.4. CNT diameter versus 3-dB bandwidth/power

Table I. Device Parameter of a CNFET

CNFET parameter	Value
Physical channel length (Lch)	32nm
Length of doped CNT source/drain extensions	32nm
Diameter of CNT	0.9nm
Gate dielectric	HfO_2
Dielectric constant	16
Chirality of tube	(11, 0)
tox	4nm
Pitch	20nm

Table 2. Device Parameter of MEMRISTOR

MEMRISTOR parameter	Value
ON resistance	1k
OFF resistance	10k
p (positive integer)	1
Average Dopant Mobility μ_V	$10^{-14}\ m^2 s^{-1} V^{-1}$
Total width of memristor 'D'	10nm

4.1 Low voltage Operation and reduced Power Consumption

The proposed multiplier circuit is operated at input supply voltage of ±0.3V. This shows that the circuit is capable of low voltage operation and hence low power consumption of the circuit can be achieved. This low voltage operation of the proposed circuit is due to the use of single stacked transistor along with a memristor connected load unlike the other low voltage mode multipliers that use double stacked transistors [4][5][19]. Thus, it can be operated at a voltage as low as ±0.3V with moderate linearity.

Fig. 5 and Fig. 6 show the power consumption of the proposed circuit for input supply voltage and input voltage respectively. The power consumption of the circuit can be as low as 43.8 μW corresponding to the inputs of 0.1V (V1 and V2) at ±0.3V power supply. These features of the proposed circuit make it suitable for battery operated portable devices especially for biomedical applications.

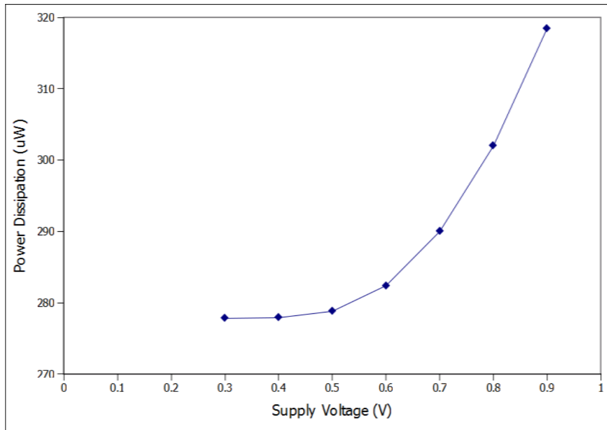

Fig.5. Power dissipation with supply voltage

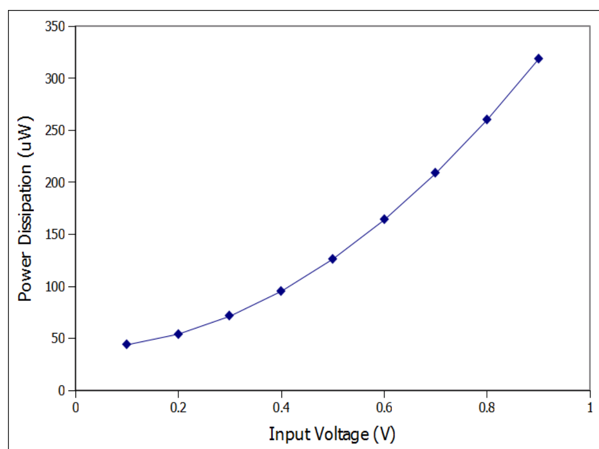

Fig.6. Power dissipation with input voltage

4.2 DC transfer characteristics

Fig.7 shows simulated DC transfer characteristics of the proposed multiplier, when V1 was swept continuously from -0.3V to 0.3V while V2 was varied from -0.3V to 0.3V with 60mV step size. It can be observed that the linear range of the circuit is approximately ±0.25V.

4.3 Frequency Response

To measure the frequency characteristics of multiplier, the proposed circuit is operated in frequency doubler configuration. A Sine wave of 0.1V peak value is given as inputs to both V1 and V2. Fig. 8 shows the typical frequency response curve. It is observed that the high-3DB frequency of 30.5 GHz is obtained from the simulated curve. This high bandwidth is attributed to the use of memristors as voltage divider elements and also to the low intrinsic capacitance of the CNFET as compared to the bulk CMOS [6] [7].

4.4 Harmonic Distortion Analysis

Fig.9 depicts the transient response of the multiplier in frequency doubler configuration. In this configuration, a 0.1V amplitude sinusoidal signal of 1MHz frequency is given as input to both V1 and V2. The harmonic distortion analysis is then performed. Figure 10 shows the variation of THD as a percentage of the output for different values of input. The simulated maximum THD is about 0.75% with a input range of ±0.25V.

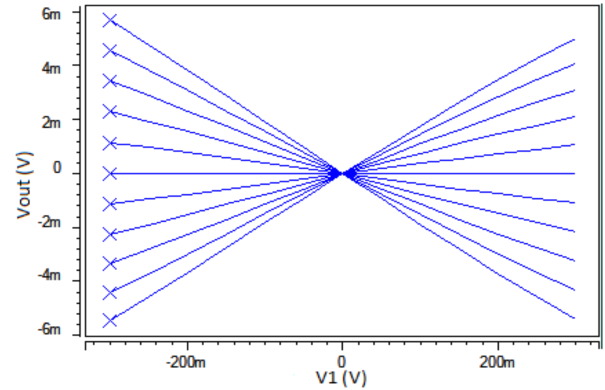

Fig.7. DC Transfer Characteristics

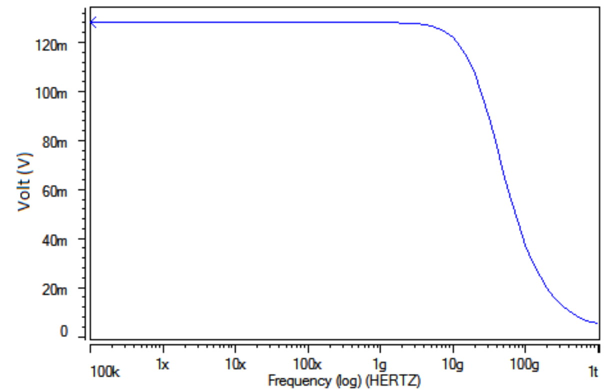

Fig.8. Frequency Response

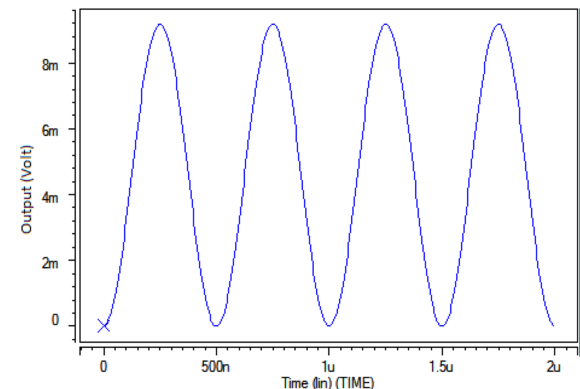

Fig. 9 Transient Response

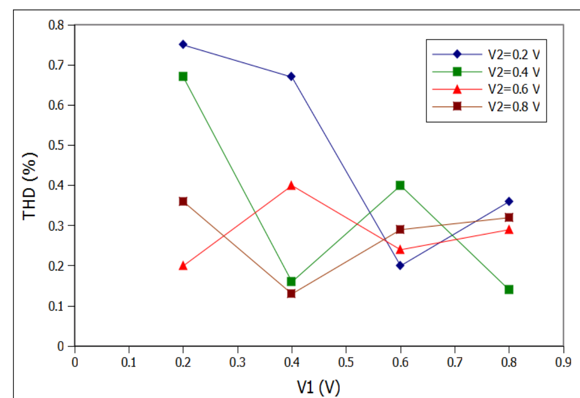

Fig.10. THD output Variation with inputs of multiplier

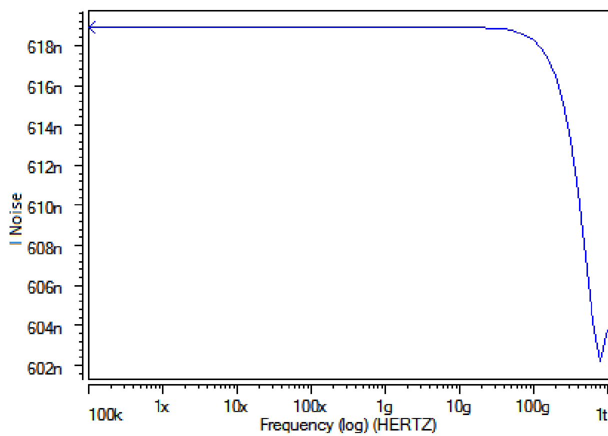

Fig.11. Equivalent input noise in (V/√Hz)

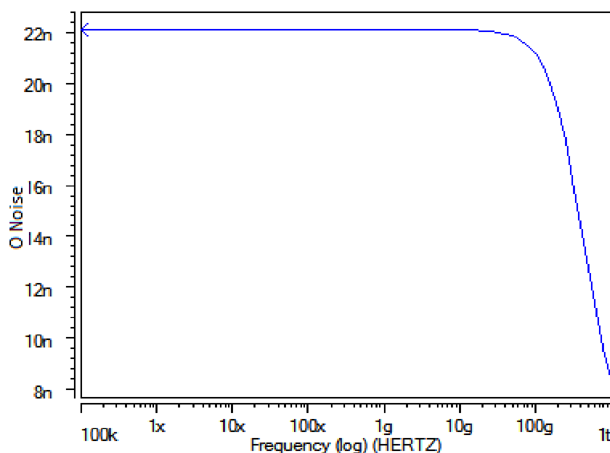

Fig.12. Equivalent output noise in (V/√Hz)

4.5 Noise Analysis

The equivalent input and output noise simulation is performed with the input sine wave of 0.1V in the frequency doubler configuration of the proposed multiplier. The results are plotted in Fig. 11 and Fig. 12 respectively. The results are in good agreement showing significant suppression of noise. The proposed multiplier uses minimal number of devices and this results in significant noise suppression.

4.6 Proposed multiplier as Amplitude Modulator

An important application of the proposed multiplier is the use of the circuit as amplitude modulator. Sinusoidal inputs of 0.1V are applied at the two inputs V1 at 1MHz and V2 at 10MHz respectively. Fig. 13 shows the modulation performance.

4.7 Comparison with previous implementations

Table 3 summarizes the comparison of the proposed multiplier with other previous work on CMOS and CNFET based multipliers. The 32nm CMOS multiplier performance parameters are also listed for better comparison. The proposed multiplier is found to be better in most of its performance measures as compared to the others. Depending upon applications, there is a trade-off between certain parameters.

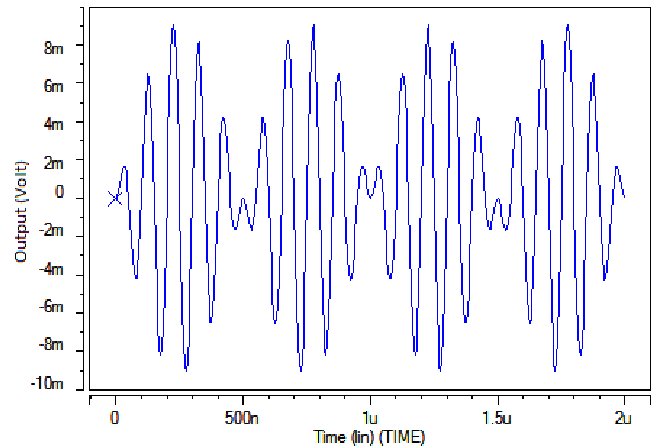

Fig.13. Amplitude Modulation Waveform for 0.1V 1MHz input and 10MHz carrier

5. CONCLUSION

This paper presents a reconfigurable differential four quadrant analog multiplier based on memristors and carbon nanotubes FETs which is capable of high bandwidth and low power operation.

The proposed circuit does not claim to be better in all respect than the others in the literature. Rather it determines how well this circuit can be used for low power applications without sacrificing its bandwidth and linearity. Extensive simulations using optimized CNFET and memristor models have proved the superior performance of most of the parameters of this multiplier in comparison to the other CMOS and CNFET based multipliers thus, making it suitable for low power applications.

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7. APPENDIX

Table 3. Comparison of the Previous Work with the Proposed Work

Parameters	Proposed Work	[20]	[27] 32 nm Design	[27]	[16]	[12]
Technology node	CNFET 32nm	CNFET 32nm	CMOS 32nm	CMOS 0.35µm	CMOS 0.35µm	CMOS 0.18µm
Voltage supply	±0.3V	±0.9V	±0.9V	+1.8V	+1.5V	±1V
Transistor count	4	6	10	10	10	36
Input range	±0.25V	±0.4V	±0.25V	±0.4V	±0.4V	±0.1V
3dB bandwidth	30.5 GHz	49.88 GHz	0.7GHz	10MHz	95MHz	3.96GHz
THD% at 1MHz	≤0.75	≤ 0.45	≤0.8 at 25KHz	≤1.0 at 25KHz	≤1.0	≤1.0
Power consumption	43.8 µW at 0.1V inputs	246.9 µW	50 µW	200µW	46.4µW	588µW