Abstract

Nowadays computers are more efficient and more complex than their predecessors. But, there is some penalty of each and every advantage in the field of technology. Here, penalty comes in terms of power consumption. According to Moore’s law, primary reasons for the rise in power consumption are the increase in clock frequency and the increased number of transistors packed onto in same die area. Reversible logic provides high speed and less power consumption. So, it has been widely used in designing of digital circuits for low-power and high-speed computation. Design of Leading One Detector (LOD) is an important circuit as they are used for the normalization process in floating point multiplication, logarithmic multiplication, and in logarithmic converters as useful components. In this paper, we designed a novel LOD based on reversible logic. In order to construct leading-one detector, the innovative reversible Feynman gate (FG) and a special case of TKS gate are proposed. The 4-bit, 8-bit, 16-bit and 32-bit LOD are designed based on the above blocks and some existing reversible gates. VHDL programmed for LOD have been modeled. According to the simulation results, our circuit’s logic structures are validated. In terms of Ancillary inputs, garbage outputs quantum cost and delay
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are compared with the reported works. It can be concluded that our designs perform better than the others. There is no doubt that these can be used as an important component the upcoming low-power quantum computing systems.

References

Implementation of Leading One Detector based on Reversible Logic for Logarithmic Arithmetic


Index Terms

Computer Science

Algorithms

Keywords

Leading one detector, Reversible logic, Feynman gate, TSK gate, Quantum computing.