Performance Investigation of a Single-phase Reduced Switched Count Multilevel Inverter with Switched DC Sources

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ABSTRACT
This paper evaluates and analyses the performance investigation of symmetrical single phase reduced switched count multi-level inverter based on switched dc source. The performance evaluation of multilevel inverter is carried out by Phase Opposition Disposition (POD) Pulse Width Modulation (PWM) technique. This approach results in reduced total harmonic distortion (THD) as compare to other PWM techniques at the output. Simulation has been carried out for various modulation indices using MATLAB/Simulink model and results have been verified

General Terms
Multi-level Inverter

Keywords
Pulse Width Modulation (PWM), Phase Opposition Disposition (POD) and Total Harmonic Distortion (THD).

1. INTRODUCTION
With the recent advancement in power electronics, multi-level emerged as one such converter whose usage has recently been seen tremendous growth in industry and utility networks with high efficiency and low cost. Its key role of dominant component in power grid, where inverters are required for renewable generation and energy saving applications can't be neglected. A MLI is structure of multiple dc level either they are (input dc source or capacitors) and power semiconductor switches connected across them. Harmonics in the multilevel inverter are better as compare to conventional two level inverter. Moreover, other advantages are reduced dv/dt on the load tend to reduce electromagnetic interference (EMI) and low voltage rating device can be employed [1-5].

The power quality of an MLI can be increased by increasing the number of levels but it leads to an increase in number of power switches thus gate drive circuits are also increased. This in turn increases the complexity to control the switches and increasing component cost. So, for practical application it is required to reduce the number of switches and gate drive circuit considerations. Moreover, lower power quality in power system network introduced many problems such as voltage sag, swell, under voltage, overvoltage, transients, flickering, harmonics etc. The main cause of harmonics in the power system is due to solid state devices i.e. non-linear devices [5-6]. However it is of major concern to opt most effective method to minimize.

This research evaluates the performance on a five level inverter with reduced switch count, isolated DC sources which are connected in alternate direction through power switches. The main purpose is to achieve improved output voltage waveform (staircase) with less switching losses and reduced THD [6-10].

In this paper, MLI is simulated through MATLAB/Simulink using POD technique. This paper is organized as. Section II shows the overall structure of MLI topology with operating modes. Phase opposition disposition control scheme based on multi carrier pulse width modulation (PWM) described in Section III. Performance investigation along with the results is shown in Section IV. Conclusion is sum up in the last Section i.e. V.

2. SYMMETRICAL REDUCED DEVICE COUNT MULTILEVEL INVERTER

2.1 Circuit Topology
The circuit diagram of symmetrical dc switched MLI topology is shown in Fig.1 [2].

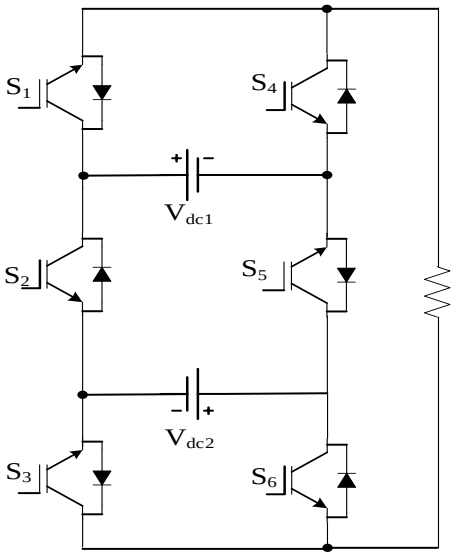

Fig.1 Symmetrical Structure of the Multilevel Inverter

The structure of single phase five level inverter consists of two isolated input dc sources namely Vdc1 and Vdc2. The two sources are connected to each other in opposite polarity through each pair of power switches. The switches used are Insulated Gate Bipolar Junction Transistor (IGBT) with antiparallel diodes. The MLI is operated with resistive load. The circuit has five valid operating modes one for each level of output voltage shows in Fig.2 to Fig.6 and these modes are summarized in Table I. These operating modes generate positive, negative and zero voltage levels.

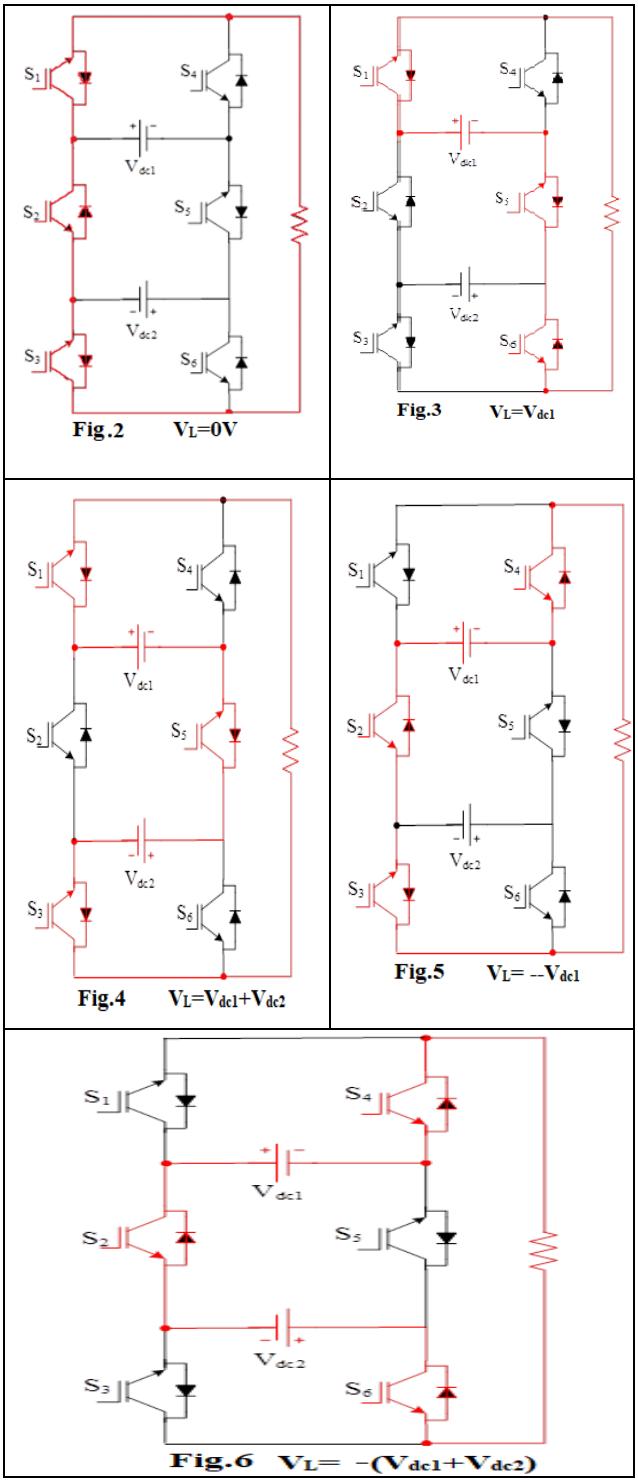

Fig. 2-6: Sustainable operating conditions for the MLI as implemented in MATLAB/SIMULINK

TABLE 1. Valid operating conditions, switching states and output voltages for the employed symmetric MLI with two input sources

Mode	Switch States						Output Voltages $v_L(t)$
	S_1	S_2	S_3	S_4	S_5	S_6	
1	OFF	OFF	OFF	ON	ON	ON	0
2	ON	OFF	OFF	OFF	ON	ON	V_{dc1}
3	ON	OFF	ON	OFF	ON	OFF	$V_{dc1}+V_{dc2}$
4	OFF	ON	ON	ON	OFF	OFF	$-V_{dc1}$
5	OFF	ON	OFF	ON	OFF	ON	$-(V_{dc1}+V_{dc2})$

2.2 Development of Simulation Model of the MLI Topology

The simulation model of DC switched MLI is shown in Fig.7. It is shown that six gate drive circuits are required for each switch and if number of sources increased to increase the output voltage level we can calculate the output levels using equation 1.

$$N = (2n + 1) \quad (1)$$

and, the maximum voltage gain for this circuit is given by

$$V_{max} = nV_{dc}. \quad (2)$$

Where 'n' is the number of sources

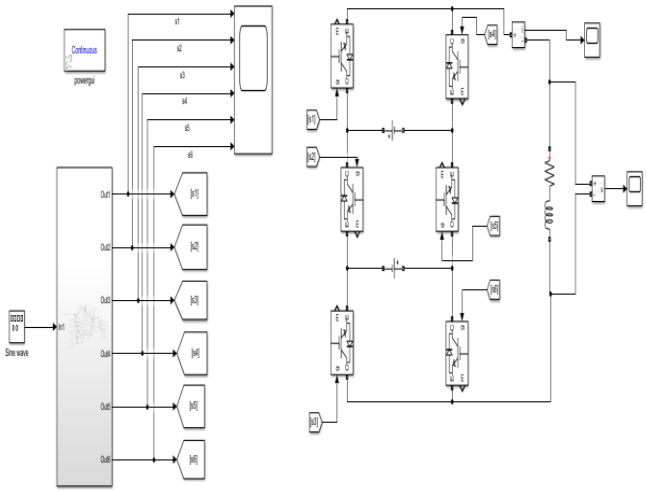

Fig.7: Simulation model of the MLI with two input dc sources

3. PHASE OPPOSITION DISPOSITION

The phase opposition disposition technique is used for the controlling output voltage of five level MLI. This controlling scheme is selected because it provides better harmonic spectrum at the output among other PWM techniques. So, in this controlling scheme, if there are five levels in output voltage of MLI then there will be four carrier signals required shown in Eq(3). For 'n' level inverter, (n-1) carrier will be required. The carrier above the zero reference will be in phase with each other and below the zero reference they are shifted by 180^0(inverted). In this scheme for MLI, the carrier frequency is 1-KHz each reference signals contain 50-Hz frequency [11-16].

$N_{carrier}$= number of levels -1 (3)

During the comparison of the reference and the carrier, when the reference is greater than the carrier above zero reference the comparator gives "n" where (n=1,2) otherwise, it gives (n-1). If the reference is greater than the carrier below zero reference, the output of comparator is "(1-n)" elsewhere, it output is "-n". Now the signals being MUX to obtain the resulting signal as shown in the Fig.8. The same controlling scheme is implemented on MATLAB/Simulink to get the five level output voltages. The waveform of POD is shown in Fig.9. The input sources Vdc1 and Vdc2 are of 24V each. The switching pulses obtained for the power switches in this circuit are shown in Fig.10.

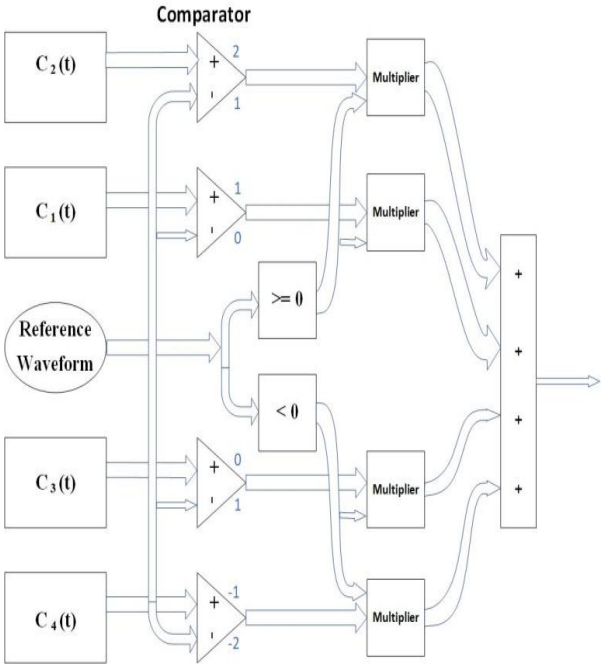

Fig.8 Switching technique for MLI

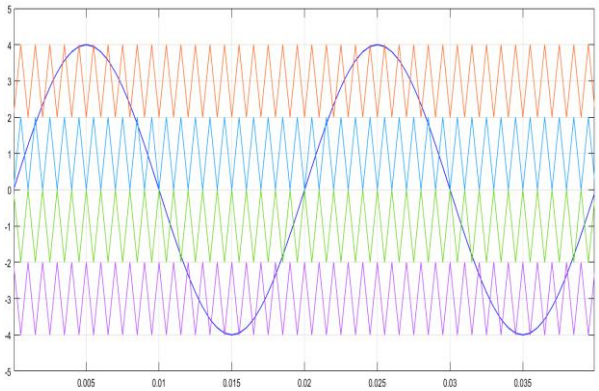

Fig.9 One Reference and Four carrier waveforms generated for employment of Five Levels MLI POD PWM technique

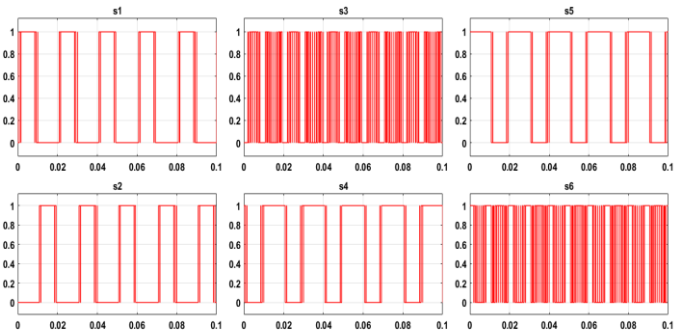

Fig.10 Switching pulses for all the Power MOSFETS i.e switches

4. PERFORMANCE INVESTIGATION AND DISCUSSION OF RESULTS

The output voltage waveform and harmonic spectrum of five levels MLI are shown in the Fig.11 and Fig.12 respectively. Note that the staircase waveform is in the step of 24V each and the maximum voltage attained is 48V according to Eq(2). From the harmonic spectrum it is shows Total Harmonic Distortion (THD) is 21.44%.

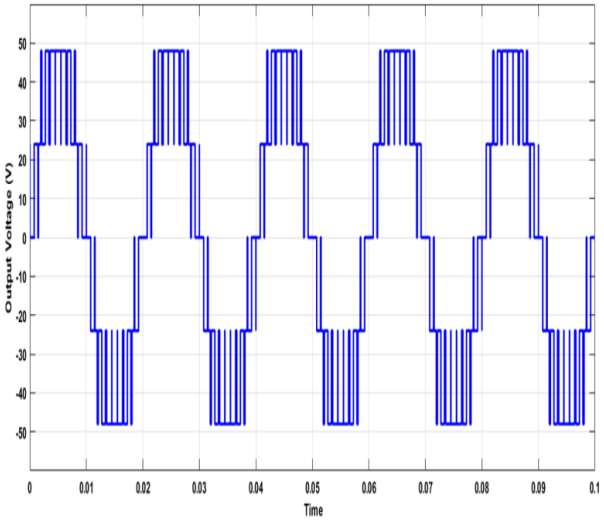

Fig.11 Five level output voltages of the MLI

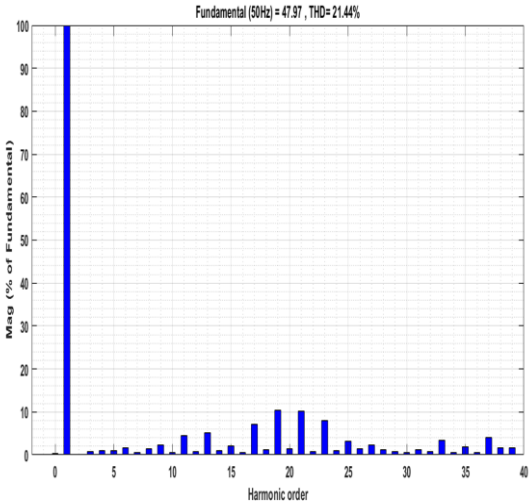

Fig.12 Harmonic Spectrum or FFT analysis

5. CONCLUSION

A five level reduced device count dc switched MLI with POD multicarrier PWM technique is successfully simulated on MATLAB/Simulink and results are presented. The simulation result shows that 21.44%. THD is produced in output voltage waveform. This THD can be further improved by increasing the number of levels in output voltage. This required more solid state switches and dc sources. In future, this work can be extended from single phase to multi-phase MLI. Moreover, utilizing different voltage sources would be beneficial rather than equal.

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