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Universal Set of Reversible Quaternary Logic Gates

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ABSTRACT

Reversible computing is of great interest due to the fact that the next generation of high performance computers must decrease heat dissipation in order to be practical, and irreversible gates dissipate energy into the environment because of the loss of information. This paper takes advantage of Multiple Valued Logic (MVL) quaternary universal set, that reduces integrated circuits (IC) interconnections, decreasing IC area, and with reversible gates that minimizes IC dissipation. The reversible computation permits both forward and backward computations, keeping the information entropy constant and decreasing heat dissipation, according to Landauer principle. The reversible gates are designed as an extension of the set of gates: Extended AND (eAND$_i$: eAND$_1$, eAND$_2$, eAND$_3$), Maximum (MAX) and Successor (SUC) already proposed in the literature. The voltage mode gates are implemented by means of three cascaded subsystems: the first subsystem discriminates 0,1,2,3 logical levels; the second subsystem performs the logic to implement each operator functionality; and the third subsystem set the right voltage output corresponding to 0,1,2,3 logical levels. Simulations with only 25, 18, 32, 10 and 32 CMOS transistors, respectively, utilizing Austriamicrosystems^{TM} technology with Cadence Virtuoso^{TM} tool demonstrate correct circuit behavior. These implementations present, for the irreversible circuits presented in the literature, fewer number of transistors.

Keywords

Reversible Computing, Universal Quaternary Set, Multiple Valued Logic

1. INTRODUCTION

Power consumption is a fundamental factor that must be addressed to build high performance systems. Among the possible paths to cope with this issue are: quantum (reversible) computing, classic reversible computing, nanotechnology, dark silicon concept, Multiple Valued Logic (MVL).

Quantum computing first discussed by Feynman [1] leads to the utilization of superposition and entanglement to perform reversible computation. In [2] the authors make a design of quantum Feynman and Toffoli gates with analysis of energy dissipation and in [3] an MVL circuit using Fredkin gates as a computational circuit suitable for reversible quantum computing is proposed. In [4] the synthesis of reversible gates in sequential circuits is proposed and nanotechnology is addressed in [5, 6] and the dark silicon concept is discussed in [7].

Quantum or classic reversible computing permits both forward and backward computations and aids to decrease energy dissipation by keeping constant entropy. In [8–11] the reversible computation is addressed. The optimization in reversible sequential circuits is proposed in [12, 13] and a methodology to the design of reversible circuits is shown in [14]. In [15] the reversible logic is demonstrated with adiabatic CMOS transistors and in [16] the reversible logic with the minimum of garbage signals is shown. In [17] the reversible logic is proposed using the adiabatic logic. Additional developments, addressed in [18], show the synthesis of reversible circuits based on Exclusive OR gate sum of products and [19] shows the implementation of reversible gate using the transistor with XOR Gate. An implementation at the transistor level for reversible digital circuit is found in [20] and [21] demonstrates a new reversible 2:4 decoder design. Design, synthesis, applications and state of the art in reversible gates are illustrated in [22, 23].

Multiple Valued Logic (MVL) allows the synthesis of digital circuits by increasing the domain to quaternary $D = \{0, 1, 2, 3\}$ digital representation. The MVL idea was introduced by Post [24] and Lukasiewicz [25] for the ternary algebra, with further developments in [26] that discuss the status of the MVL. Note that a quaternary digit corresponds to two binary bits. MVL decreases the number of interconnections, pads and power consumption, as well as the total area of the Integrated Circuit (IC), as the interconnections are about 70% of the total area [27,28]. In [29] the MVL universal set of operators for any B base, that is, an algebra, minimization tools and synthesis methodology, is presented. In [30] a universal set of CMOS ports for the synthesis of digital logic circuits of multiple values is presented and a quaternary analog to digital converter application is addressed in [31]. Design based on ternary logic can be seen in [32].

All the above technologies help to cope with the energy issue and, in this environment, the purpose of this work is to demonstrate functional correctness and CMOS circuits feasibility through simulations of the combination of the MVL technique with classical reversible gates. Therefore, this work proposes the design and simulation of quaternary reversible gates that keeps the information entropy constant in the system, implying a bijective mapping between input and output, that decreases heat dissipation, according to Landauer principle [33]. This is due to the fact that, for one bit loss of information, that happens in each AND, OR gate of the combinational circuits, $KTln2$ Joules of energy are dissipated, where K stands for Boltzmann's constant (1.3807 $\times$ 10^{-23} Joules per Kelvin) and T is the absolute temperature, ln is the natural logarithm and the number 2 comes from the binary base. The non-reversible universal quaternary set of gates, already presented in the literature: Successor (SUC), Extended

AND ($eAND_1$, $eAND_2$, $eAND_3$), and Maximum (MAX) [30] is further extended to include the reversible characteristic by means of a bijective mapping that performs forward and backward computation with the same gate. Among the many ways to define the bijective mapping it is here presented one alternative. The actual implementation is based on three subsystems the first one discriminates each logical level, the second performs the logical steps to implement the gate under consideration and the third set the logical output level. Simulations with CMOS transistors utilizing Austriamicrosystems™ technology with Cadence Virtuoso™ tool demonstrate feasibility of the circuits and correct reversible quaternary computing behavior, additionally, the non-reversible gates have fewer number of transistors (only 25, 18, 32, 10 and 32 MOS transistors, for the $eAND_i$, MAX, SUC, respectively) that is better than [30] in terms of transistors counting.

The rest of this paper is organized as follows: Section 2 defines the MVL reversible primal algebra; Section 3 addresses the MVL operators CMOS implementation; Section 4 presents results and the discussion and finally; Section 5 summarizes the concluding remarks and future work.

2. MVL REVERSIBLE PRIMAL ALGEBRA

For notation purposes SUC, $eAND_i$, MAX [29] and SUC_r, $eAND_ir$, MAX_r denote non-reversible and reversible gates defined here, respectively. SUC is an unary (i.e. one operand) operator and $eAND_i$, MAX are binary operators (i.e. two operands).

The non-reversible universal quaternary set of gates is defined in the cyclic ordered domain D:{0,1,2,3} as follows:

Let i, inputs: VinA, VinB, and the outputs: SUC, $eAND_i$, MAX $\in$ D:{0,1,2, 3}.

$eAND_i$ definition: if VinA=VinB=i then $eAND_i$=i, otherwise $eAND_i$=0.

MAX definition: if VinA$\geq$VinB then MAX=VinA, otherwise MAX=VinB.

SUC definition: if VinA=i then SUC=(i+1) Mod 4. Where Mod stands for the Modulo operation.

There are many ways to define the bijective mapping that performs forward and backward computation and it is up to the designer to choose one.

For two inputs reversible operators implementations, as shown in Tables 1, 2, 3, 4 there exist three inputs: two operator inputs (VinA,VinB) and one ancillary input (VinC); and three outputs: the operator output ($eAND_{ir}$ or MAX_r) and two garbage outputs (g_{Br},g_{Ar}). For one input reversible operator implementation, as shown in Table 5 there exists two inputs: one operator input (VinA) and one ancillary input (VinC) and two outputs: one operator output (SUC_r) and one garbage output (g_{Ar}).

Table 1. eAND$_{3r}$ direct → inverse

Vin_C	Vin_B	Vin_A	eAND3$_r$	g_{Br}	g_{Ar}		Vin_C	Vin_B	Vin_A	eAND3$_r$	g_{Br}	g_{Ar}
ancillary							eAND3$_r$	g_{Br}	g_{Ar}	Vin_C	Vin_B	Vin_A
0	0	0	0	0	0	→	0	0	0	0	0	0
0	0	1	0	0	1	→	0	0	1	0	0	1
0	0	2	0	0	2	→	0	0	2	0	0	2
0	0	3	0	0	3	→	0	0	3	0	0	3
0	1	0	0	1	0	→	0	1	0	0	1	0
0	1	1	0	1	1	→	0	1	1	0	1	1
0	1	2	0	1	2	→	0	1	2	0	1	2
0	1	3	0	1	3	→	0	1	3	0	1	3
0	2	0	0	2	0	→	0	2	0	0	2	0
0	2	1	0	2	1	→	0	2	1	0	2	1
0	2	2	0	2	2	→	0	2	2	0	2	2
0	2	3	0	2	3	→	0	2	3	0	2	3
0	3	0	0	3	0	→	0	3	0	0	3	0
0	3	1	0	3	1	→	0	3	1	0	3	1
0	3	2	0	3	2	→	0	3	2	0	3	2
0	3	3	0	3	3	→	0	3	3	0	3	3

Table 2. eAND$_{2r}$ direct → inverse

Vin_C	Vin_B	Vin_A	eAND2$_r$	g_{Br}	g_{Ar}		Vin_C	Vin_B	Vin_A	eAND2$_r$	g_{Br}	g_{Ar}
ancillary							eAND2$_r$	g_{Br}	g_{Ar}	Vin_C	Vin_B	Vin_A
0	0	0	0	0	0	→	0	0	0	0	0	0
0	0	1	0	0	1	→	0	0	1	0	0	1
0	0	2	0	0	2	→	0	0	2	0	0	2
0	0	3	0	0	3	→	0	0	3	0	0	3
0	1	0	0	1	0	→	0	1	0	0	1	0
0	1	1	0	1	1	→	0	1	1	0	1	1
0	1	2	0	1	2	→	0	1	2	0	1	2
0	1	3	0	1	3	→	0	1	3	0	1	3
0	2	0	0	2	0	→	0	2	0	0	2	0
0	2	1	0	2	1	→	0	2	1	0	2	1
0	2	2	2	2	2	→	2	2	2	0	2	2
0	2	3	0	2	3	→	0	2	3	0	2	3
0	3	0	0	3	0	→	0	3	0	0	3	0
0	3	1	0	3	1	→	0	3	1	0	3	1
0	3	2	0	3	2	→	0	3	2	0	3	2
0	3	3	0	3	3	→	0	3	3	0	3	3

Table 3. eAND$_{1r}$ direct → inverse

Vin_C	Vin_B	Vin_A	eAND1$_r$	g_{Br}	g_{Ar}		Vin_C	Vin_B	Vin_A	eAND1$_r$	g_{Br}	g_{Ar}
ancillary							eAND1$_r$	g_{Br}	g_{Ar}	Vin_C	Vin_B	Vin_A
0	0	0	0	0	0	→	0	0	0	0	0	0
0	0	1	0	0	1	→	0	0	1	0	0	1
0	0	2	0	0	2	→	0	0	2	0	0	2
0	0	3	0	0	3	→	0	0	3	0	0	3
0	1	0	0	1	0	→	0	1	0	0	1	0
0	1	1	1	1	1	→	1	1	1	0	1	1
0	1	2	0	1	2	→	0	1	2	0	1	2
0	1	3	0	1	3	→	0	1	3	0	1	3
0	2	0	0	2	0	→	0	2	0	0	2	0
0	2	1	0	2	1	→	0	2	1	0	2	1
0	2	2	0	2	2	→	0	2	2	0	2	2
0	2	3	0	2	3	→	0	2	3	0	2	3
0	3	0	0	3	0	→	0	3	0	0	3	0
0	3	1	0	3	1	→	0	3	1	0	3	1
0	3	2	0	3	2	→	0	3	2	0	3	2
0	3	3	0	3	3	→	0	3	3	0	3	3

For all operators, VinC controls direct (VinC equals to 0 level) or reverse computation (VinC equals to non 0 level). The outputs g_{Br}, g_{Ar} are utilized in order to not repeat any possible code making the mapping invertible. Therefore, they are not useful for any other purpose except the invertibility. Of course, it is possible to utilize these output to define other operators, but for the purpose in this work, there is not any utility to implement that and if implemented it would increment further the complexity of the electronic circuits. To control forward and backward computation with the same gate, they are connected as shown in Figure 1 in which VinC equals 0 level performs the direct and VinC equals to non 0 level performs the inverse computation. VinB, VinA are the operators' inputs. To reverse the operator each output of the direct gate computation:

Table 4. MAX$_r$ direct → inverse

Vin_C	Vin_B	Vin_A	MAX$_r$	g_{Br}	g_{Ar}		Vin_C	Vin_B	Vin_A	MAX$_r$	g_{Br}	g_{Ar}
ancillary							MAX$_r$	g_{Br}	g_{Ar}	Vin_C	Vin_B	Vin_A
0	0	0	0	0	0	→	0	0	0	0	0	0
0	0	1	1	0	1	→	1	0	1	0	0	1
0	0	2	2	0	2	→	2	0	2	0	0	2
0	0	3	3	0	3	→	3	0	3	0	0	3
0	1	0	1	1	0	→	1	1	0	0	1	0
0	1	1	1	1	1	→	1	1	1	0	1	1
0	1	2	2	1	2	→	2	1	2	0	1	2
0	1	3	3	1	3	→	3	1	3	0	1	3
0	2	0	2	2	0	→	2	2	0	0	2	0
0	2	1	2	2	1	→	2	2	1	0	2	1
0	2	2	2	2	2	→	2	2	2	0	2	2
0	2	3	3	2	3	→	3	2	3	0	2	3
0	3	0	3	3	0	→	3	3	0	0	3	0
0	3	1	3	3	1	→	3	3	1	0	3	1
0	3	2	3	3	2	→	3	3	2	0	3	2
0	3	3	3	3	3	→	3	3	3	0	3	3

Table 5. SUC$_r$ direct → inverse

Vin_C	Vin_A	SUCr	g_{Ar}		Vin_c	Vin_a	SUCr	g_{Ar}
ancillary					SUC$_r$	g_{Ar}	Vin_C	Vin_A
0	0	1	0	→	1	0	0	0
0	1	2	1	→	2	1	0	1
0	2	3	2	→	3	2	0	2
0	3	0	3	→	0	3	0	3

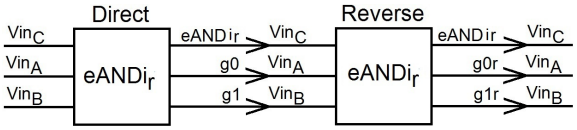

Fig. 1: eAND$_{ir}$ direct and eAND$_{ir}$ reverse block diagram connection

$eAND_{ir}$ or MAX_r or SUC_r is connected to the input VinC of the reverse gate computation, g_{Br} is connected to VinB and g_{Ar} is connected to VinA for the binary operators and only g_{Ar} is connected to VinA for the unary operator (SUC_r).

3. MVL OPERATORS CMOS IMPLEMENTATION

All CMOS operators' implementation description is based on three subsystems and is presented based on the Figures in block diagrams and CMOS gates circuits. In all Figures, at the top, the circuit that is focused on the gates' implementation at the input/output $voltage$ level along with the algorithms describing the gates' implementation, is shown. At the bottom, the block diagram that is focused on the input/output $logical$ level along with the logical equations describing them, is also shown. All gates utilize the discriminators (first subsystem) to verify the logical level input; the binary logic circuit (second subsystem) implements the logic of the particular level under consideration; and finally, the multiplexers or switches (third subsystem) set the output to the right voltage level. For example, the $eAND_3$ gate demands that both inputs are set to the 3 logical level. Then, the discriminators (first subsystem) verify these conditions, the binary logic circuit (second subsystem) verifies the intersection in the 3 level, that is, both inputs are set to the 3 logical level simultaneously; and finally, the multiplexers (third subsystem) set the output to the right voltage level (3V). All others gates follow the same design criteria, as presented next.

Note that the logical levels are defined as: (ground) 0V is the 0 logical level, 1V is the 1 logical level, 2V is the 2 logical level, (VDD) 3V is the 3 logical level. However, if in the middle of the circuit a particular gate output is set to 3V, it does not always mean the 3 logical level, it only means that the output is high voltage (because it is binary), by looking at the circuit gate and the block diagram the actual situation is clear by the context.

For the logic implementation the INV (inverter), NAND, NOR binary gates are utilized and they are represented as in the binary logic with a number inside that defines the threshold voltage (Vth) utilized to discriminate the quaternary logical levels. Whenever there is not any number inside, the Vth is set to 1.5V (middle of VDD=3V polarization voltage of the gate). In the following, two criteria are needed. First, for all gates, first subsystem discriminates which logical level (0,1,2,3) is at the input by comparing each input (VinC, VinB, VinA) with corresponding threshold Vth values (0.7V, 1.4V, 2.2V), as shown in Figure 2, defined by setting the CMOS width and length sizes.

The implementation utilizes binary levels, that is, all these gates always discriminate between two subsets, as for example, 0 level from 1,2,3 levels or 0,1 levels from 2,3 levels, etc. As shown in

Table 6. Algorithms table

Algorithm 1	Algorithm 2	Algorithm 3
INV$_{Vth}$	NAND$_{Vth}$	NOR$_{Vth}$
If VinA $\leqslant$ Vth	If (VinA AND VinB) $\leqslant$ Vth	If (VinA OR VinB) $\leqslant$ Vth
x	x	x
Else	Else	Else
y	y	y
EndIf	EndIf	EndIf

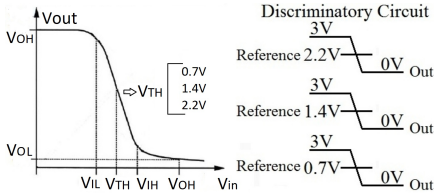

Fig. 2: MVL thresholds of the discriminators

the Algorithm 1 in Table 6, INV$_{0.7V}$(VinA) discriminates between subsets x=0 logical level from y=1,2,3 logical levels, when its input (VinA) is less than 0.7V (in the gate circuit, the output is 3V); INV$_{1.4V}$(VinA) discriminates between subsets x=0,1 logical levels from y=2,3 logical levels, when its input (VinA) is less than 1.4V (in the gate circuit, the output is 3V); INV$_{2.2V}$(VinA) discriminates between subsets x=0,1,2 logical levels from y=3 logical level, when its input (VinA) is less than 2.2V (in the gate circuit, the output is 3V); INV(VinA) discriminates to set 0V or VDD, when its input (VinA) is less than 1.5V (in the gate circuit, VDD is the polarization of the CMOS).

Second, the target of the discrimination for a given gate, i.e. what is the subset (x or y) of interest, as for example: x=0 or y=1,2,3; x=0,1 or y=2,3 and so on.

In the circuit description, in the block diagram, the logical function to implement the gate under consideration is presented, and after that, the CMOS circuit to show the actual voltages in the implementation.

For the presentation of the logical function, the name of the gate with its threshold (i.e INV$_{0.7V}$) is utilized as the name of the quaternary function corresponding to the NAND or NOR or INV in the block diagram and in the parenthesis its inputs, as shown latter.

Same criteria for the NAND and NOR binary gates in which the Vth helps to discriminate logical (x or y) levels subsets, detailed latter in the description of each operator implementation.

As shown in the Algorithm 2 in Table 6, NAND$_{Vth}$(VinB,VinA) discriminates between subsets x logical levels from y logical levels, when both of its inputs (VinB,VinA) are greater than Vth (in the gate circuit, the output is 0V, meaning that both inputs belongs to the y subset).

As shown in the Algorithm 3 in Table 6, NOR$_{Vth}$(VinB,VinA) discriminates between subsets x logical levels from y logical levels, when one of its inputs (VinB or VinA) are greater than Vth (in the gate circuit, the output is 0V, meaning that both inputs belongs to the x subset). Follows the actual gates implementation description.

3.1 $eAND_{ir}$ Implementations

3.1.1 $eAND_{3r}$ Implementation. The binary operator $eAND_{3r}$ implementation, as defined in Table 1 is shown in Figure 3. Note that columns VinB, VinA and $eAND_{3r}$ implement exactly the non-reversible $eAND_3$ operator definition. For the two operands $eAND_{3r}$ implementation, there exists three inputs (VinC, VinB, VinA) and three outputs ($eAND_{3r}$, g_{Br}, g_{Ar}). VinC (ancillary

Table 7. eAND$_{3r}$ transistors size

Transistor	W	L	Transistor	W	L
PMOS	(μm)	(μm)	NMOS	(μm)	(μm)
MP01	20	0.35	MN01	10	0.35
MP02/03	20	0.35	MN02/03	0.4	0.35
MP04	0.4	0.35	MN04	0.4	0.35
MP05	0.8	0.35	MN05	0.4	0.35

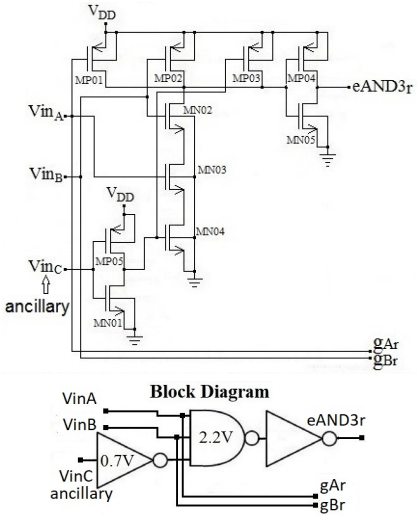

Fig. 3: eAND$_{3r}$ circuit

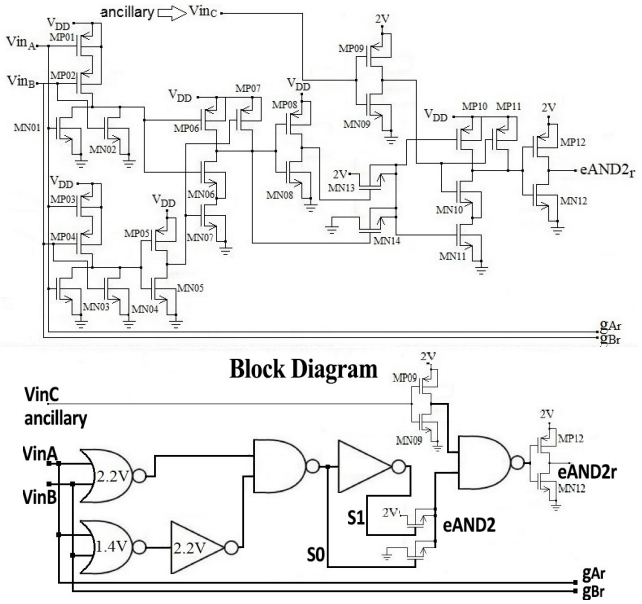

Fig. 4: eAND$_{2r}$ circuit

input) controls direct (VinC equals to 0 level) and to reverse the computation (VinC equals to non 0 level). Follows the logical function based on the operator circuit, in Equation 1.

$$eAND_{3r} = INV\{NAND_{2.2V}[VinA, VinB, INV_{0.7V}(VinC)]\} \quad (1)$$

As it can be seen in Figure 3, in this function the target of the INV with CMOS transistors (MN05,MP04) and threshold 1.5V with output $eAND_{3r}$ is to set the 3 level, when all three inputs of the NOR$_{2.2V}$ (VinA,VinB,INV$_{0,7V}$(VinC)) belong to the 3 level.
In the arguments of the function, the target of the INV$_{0.7V}$ with input VinC is to identify level 0 to control forward and backward computation with CMOS transistors (MN01,MP05). The target for the NAND$_{2.2V}$ is to identify that all inputs belong to the 3V with CMOS transistors (MN02,MP03,MN04,MP01,MP02, MN03), and therefore, this intersection defines that both VinA, VinB must have 3 logical levels. Table 7 shows the size of the CMOS transistors.

3.1.2 $eAND_{2r}$ Implementation. The binary operator $eAND_{2r}$ implementation, as defined in Table 2, is shown in Figure 4. Note that columns VinB, VinA and $eAND_{2r}$ implement exactly the non-reversible $eAND_2$ operator definition. For the two operands $eAND_{2r}$ implementation, there exists three inputs (VinC, VinB, VinA) and three outputs ($eAND_{2r}$, g$_{Br}$, g$_{Ar}$). VinC (ancillary input) controls direct (VinC equals to 0 level) and to reverse the computation (VinC equals to non 0 level). When the selector S1 equals to 2 level then $eAND2$=2V; otherwise $eAND2$=0V. Follows the logical functions based on the operator circuit, in Equation 2.

$$S1 = INV(S0) \qquad S0 = NAND\{NOR_{2.2V}(VinA, VinB), INV_{2.2V}[NOR_{1.4V}(VinA, VinB)]\} \quad (2)$$

As shown in the Figure 4 the INV with input VinC with polarization voltage of 2V controls forward (VinC=0V) and backward (VinC different from 0 level) computation with CMOS transistors (MN09,MP09).

Output $eAND_{2r}$ is set to 2 level by inverting the NAND gate if both inputs (direct computation controlled by VinC and $eAND_2$) are in the high level simultaneously, that is, $eAND_2$ output is set to 2V by activating the transistor (MN13); otherwise $eAND_{2r}$ is set to 0V by activating the transistor (MN14).
In the argument of the S0 function, NAND has two inputs: first the output of the NOR with threshold 2.2V (NOR$_{2,2V}$); second the output of the INV$_{2.2V}$ with input NOR$_{1.4V}$(VinB,VinA).
The target of the NAND is that both of its inputs are set in the 2 level by the intersection between the subsets 0,1,2 and 2,3 with CMOS transistors (MN06,MP06,MN07,MP07). The target of the NOR$_{2.2V}$ is to identify the subset 0,1,2 (setting its output to 3V) with CMOS transistors (MN01,MP01,MN02, MP02). The target for the NOR$_{1.4V}$ is to identify the subset 0,1 level (setting its output to 0V) with CMOS transistors (MN03,MP03,MN04,MP04). The next inverter INV$_{2.2V}$(NOR$_{1,4V}$(VinB,VinA)) inverts the signal to identify the subset 2,3 level (setting its output to 3V) with CMOS transistors (MN05, MP05). Table 8 shows the size of the CMOS transistors.

3.1.3 $eAND_{1r}$ Implementation. The binary operator $eAND_{1r}$ implementation, as defined in Table 3 is shown in Figure 5. Note that columns VinB, VinA and $eAND_{1r}$ implement exactly the non-reversible $eAND1$ operator definition. For the two operands $eAND_{1r}$ implementation, there exists three inputs (VinC, VinB, VinA) and three outputs ($eAND_{ir}$, g$_{Br}$, g$_{Ar}$). VinC (ancillary input) controls direct (VinC equals to 0 level) and to reverse the

Table 8. eAND$_{2r}$ transistors size

Transistor	W	L	Transistor	W	L
PMOS	(μm)	(μm)	NMOS	(μm)	(μm)
MP01/02	25	1	MN01/02	1	15
MP03/04	24	0.35	MN03/04	0.4	0.35
MP05/06/07/08	10	0.35	MN05/06/07/08	10	0.35
MP09	0.8	0.35	MN09	10	0.35
MP10/11/12	10	0.35	MN10/11/12	10	0.35
			MN13/14	2	2

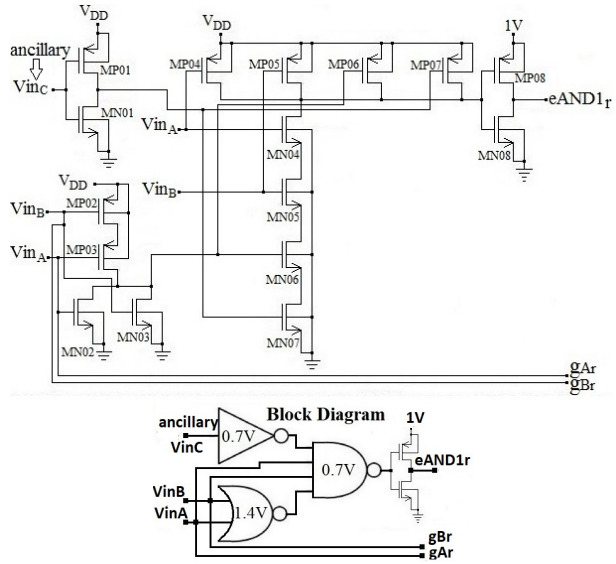

Fig. 5: eAND$_{1r}$ circuit

computation (VinC equals to non 0 level). Follows the logical functions based on the operator circuit, in Equation 3.

$$eAND_{1r} = INV\{NAND_{0.7V}[INV_{0.7V}(VinC), VinA, VinB, NOR_{1.4V}(VinA, VinB)]\} \quad (3)$$

In the argument of the $eAND_{1r}$ function, the INV with threshold 1.5V with CMOS transistors (MN08,MP08) with polarization voltage of 1V set the output to 1 level. the argument to the INV function is the (NAND$_{0.7V}$) with threshold 0.7V that has four inputs: first the output of the inverter with threshold 0.7V (INV$_{0.7V}$) that has as its input the VinC input; second the input VinA; third the VinB input; and fourth the output of the NOR with threshold 1.4V (NOR$_{1.4V}$) with inputs (VinB,VinA). The target of the INV$_{0.7V}$ it to identify level 0 to control forward and backward computation with CMOS transistors (MN01,MP01). The target of the NOR$_{1.4V}$ is to identify if both inputs belong to the 0,1 levels (NOR$_{1.4V}$ output in 3V) with CMOS transistors (MN02,MP02,MN03,MP03). The target for the NAND$_{0.7V}$ is to identify that all inputs belong to the 1,2,3 logical levels (NAND$_{0.7V}$ output in 0V) with CMOS transistors (MN04,MP04,MN05,MP05, MN06,MP06,MN07,MP07), and therefore, this intersection defines that both VinA, VinB must have 1 logical levels. The last inverter (MN08, MP08) set the $eAND_{1r}$ output to 1V, that is the $eAND_{1r}$ voltage level output. g$_{Ar}$, g$_{Br}$ are exactly the same as VinB and VinA, respectively. Table 9 shows the size of the CMOS transistors.

3.2 MAX_r Implementation

The binary operator MAX_r implementation, as defined in Table 4 is shown in Figure 6. Note that columns VinB, VinA and MAX_r implement exactly the non-reversible MAX operator definition.

Table 9. eAND$_{1r}$ transistors size

Transistor PMOS	W (μm)	L (μm)	Transistor NMOS	W (μm)	L (μm)
MP01	0.8	0.35	MN01	10	0.35
MP02/03	5	0.35	MN02/03	0.4	0.35
MP04/05/06/07	0.4	0.35	MN04/05/06/07	18	0.35
MP08	10	0.35	MN08	10	0.35

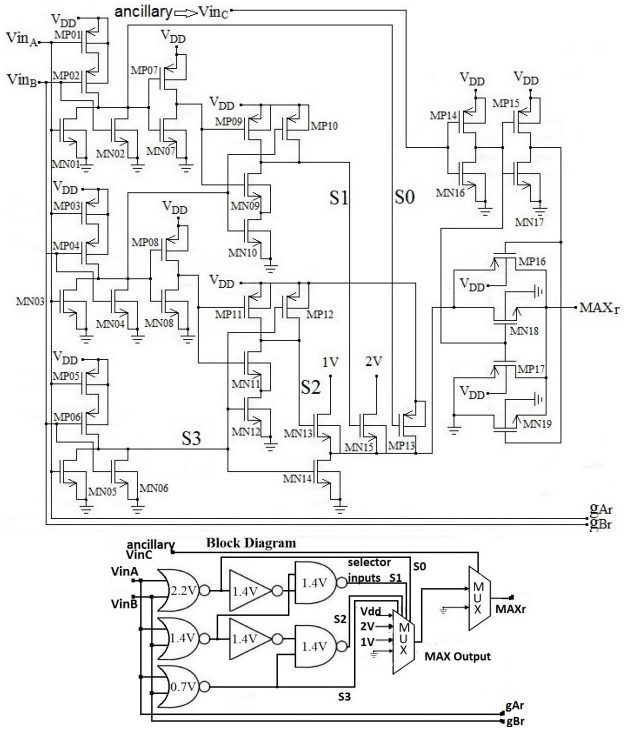

Fig. 6: MAX$_r$ circuit

For the two operands MAX_r implementation there exists three inputs, (VinC, VinB, VinA) and three outputs (MAX_r, g$_{Br}$, g$_{Ar}$). VinC (Ancillary) controls direct (VinC equals to 0 level) or reverse computation (VinC equals to non 0 level). VinB, VinA are the operators' inputs. g$_{Br}$, g$_{Ar}$ (garbage) are utilized in order to making the mapping invertible.
When VinC=0 level, the selector input of the multiplexer with output MAX_r and inputs (0V=ground and Max output) computes the forward computation; otherwise it computes the backward computation. Follows the logical functions based on the operator circuit, in Equation 4.

$$\begin{aligned} S0 &= NOR_{2.2V}(VinB, VinA) \\ S1 &= NAND_{1.4V}\{NOR_{1.4V}(VinB, VinA), \\ &\quad INV_{1.4V}[NOR_{2.2V}(VinB, VinA)]\} \\ S2 &= NAND_{1.4V}\{NOR_{0.7V}(VinB, VinA), \\ &\quad INV_{1.4V}[NOR_{1.4V}(VinB, VinA)]\} \\ S3 &= NOR_{0.7V}(VinB, VinA) \end{aligned} \quad (4)$$

The implementation criteria for the selector inputs to the quaternary multiplexer is that when one and only one of the selector inputs is different from 0 level the MAX output signal must be set to that level, otherwise it is set to the 0 level.
Therefore, if the selector input (S0=0V) generated by the NOR$_{2.2V}$ identifies the 3 level then, MAX output equals to 3 level, and all the other inputs in the selector inputs are 0 level. The target of the NOR$_{2.2V}$ is to discriminate x=0,1,2 level from y=3 level with CMOS transistors (MN01, MP01, MN02, MP02).
If the selector input (S1=3V) generated by the NAND$_{1.4V}$ identifies the 2 level then MAX output equals to 2 level, and all the other inputs in the selector inputs are 0 level. The target of the

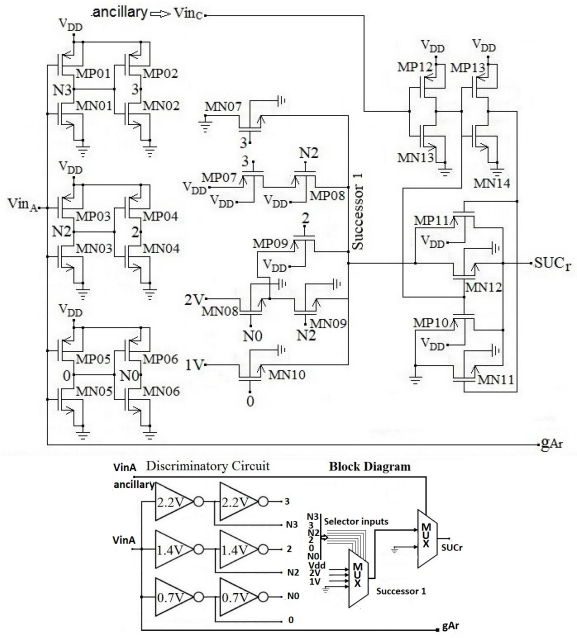

Fig. 7: SUC$_r$ circuit

NAND$_{1.4V}$ is to discriminate x=0,1 level from y=2,3 level with CMOS transistors (MN09, MP09, MN010, MP010). The target of the NOR$_{1.4V}$ is to discriminate x=0,1 level from y=2,3 level with CMOS transistors (MN03, MP03, MN04, MP04). INV$_{1.4V}$ inverts the signal with CMOS transistors (MN07, MP07).
If the selector input (S2=3V) generated by the NAND$_{1.4V}$ identifies the 1 level then MAX output is 1 level, and all the other inputs in the selector inputs are 0 level. The target of the NOR$_{1.4V}$ is to discriminate x=0,1 level from y=2,3 level with CMOS transistors (MN11, MP11, MN12, MP12). INV$_{1.4V}$ inverts the signal with CMOS transistors (MN08, MP08).
If the selector input (S3=3V) generated by the NOR$_{0.7V}$ identifies the 0 level then MAX output is 0 level, and all the other inputs in the selector inputs are 0 level. The target of the NOR$_{0.7V}$ is to discriminate x=0,1 level from y=2,3 level with CMOS transistors (MN05, MP05, MN06, MP06). Table 10 shows the size of the CMOS transistors.

3.3 SUC_r Implementation

The unary operator SUC_r implementation, as defined in Table 5 is shown in Figure 7. Note that columns VinA and SUC_r implement exactly the non-reversible SUC operator definition.
VinC inputs to the quaternary multiplexer selector with inputs Successor1 and ground (0 level) to control direct (VinC equals

Table 10. MAX$_r$ transistors size

Transistor PMOS	W (μm)	L (μm)	Transistor NMOS	W (μm)	L (μm)
MP01/02	10	0.35	MN01/02	0.4	10
MP03/04	4.4	0.35	MN03/04	0.5	0.35
MP05/06	0.4	0.35	MN05/06	10	0.35
MP07 up to 12	4.4	0.35	MN07 up to 12	2.8	0.35
MP13	5.9	2	MN13	1	1
MP14	0.8	0.35	MN14	1	1
MP15	10	0.35	MN15	1	1
MP16/17	5.9	2	MN16/17	10	0.35
			MN18/19	2	2

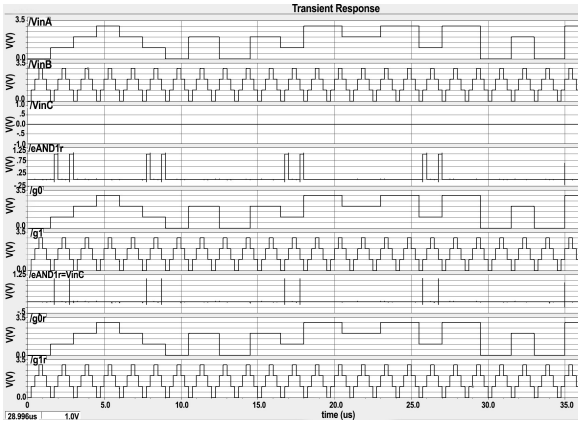

Fig. 8: eAND$_{1r}$ simulation

to 0 level, then SUC_r =Successor1) by activating the switch (MP11,MN12) to set SUC_r=Sucessor1 level through the transistors (MP12,MN13,MP13,MN14). To reverse the computation (VinC equals to non 0 level, then SUC_r=0 level) by activating the switch (MP10,MN11) to set SUC_r=0 level of the multiplexer.
The other quaternary multiplexer with signal inputs 3, N3, 2, N2, 0, N0 set Sucessor1=i as VinA=i level which level is at the input SUC_r, and then, the output SUC_r=i+1 level by means of choosing the right input from: ground (0 level), 1V (1 level), 2V (2 level), VDD (3 level). Follows the logical functions based on the operator circuit, in Equation 5.

$$\begin{aligned} 0 &= INV_{0.7V}(VinA) \quad & N0 &= INV_{0.7V}[INV_{0.7V}(VinA)] \\ 2 &= INV_{1.4V}[INV_{1.4V}(VinA)] \quad & N2 &= INV_{1.4V}(VinA) \\ 3 &= INV_{2.2V}[INV_{2.2V}(VinA)] \quad & N3 &= INV_{2.2V}(VinA) \end{aligned} \tag{5}$$

Signal 3: INV$_{2,2V}$(VinA) discriminates x=0,1,2 levels from y=3 level, with the CMOS transistors (MN01,MP01). The target is the y=3 level. Then, it identifies if VinA is in the level 3 and N3 identifies that is in the x=0,1,2 levels (N3=Not 3), with the CMOS transistors (MN02,MP02). Signal 2: INV$_{1,4V}$(VinA) discriminates x=0,1 levels from y=2,3 level, with the CMOS transistors (MN03,MP03). The target is the y=2,3 level. Then, it identifies if VinA is in the level y=2,3 and N2 identifies that is in the x=0,1 levels (N2=2,3), with the CMOS transistors (MN04,MP04). Signal 0: INV$_{0,7V}$(VinA) discriminates x=0 levels from y=1,2,3 level, with the CMOS transistors (MN05, MP05). The target is the y=1,2,3 level. Then, it identifies if VinA is in the level y=1,2,3 and N0 identifies that is in the x=0 levels (N0=Not 0), with the CMOS transistors (MN06,MP06). The multiplexer utilizes the selector inputs to set only one input of the selector in the level 0 or 1 or 2 or 3, that is the purpose of the negation of each signal 3,2,0 that aid to control the switches in the multiplexer. Signal 3 controls switch (MN07) to set Sucessor1=3 level (when VinA=2, SUC_r=3); signal

Table 11. SUC$_r$ transistors size

Transistor PMOS	W (μm)	L (μm)	Transistor NMOS	W (μm)	L (μm)
MP01/02	15	0.35	MN01/02	0.4	4
MP03/04	8.3	0.35	MN03/04	2.8	0.35
MP05/06	0.8	0.35	MN05/06	10	0.35
MP07 up to 11	0.4	0.35	MN07 up to 11	0.4	0.35
MP12	0.8	0.35	MN12	0.4	0.35
MP13	10	0.35	MN13/14	10	0.35

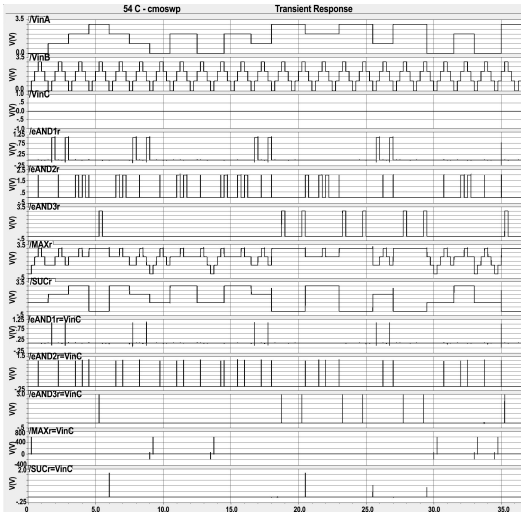

Fig. 9: Gates simulation 54°C cmostm model

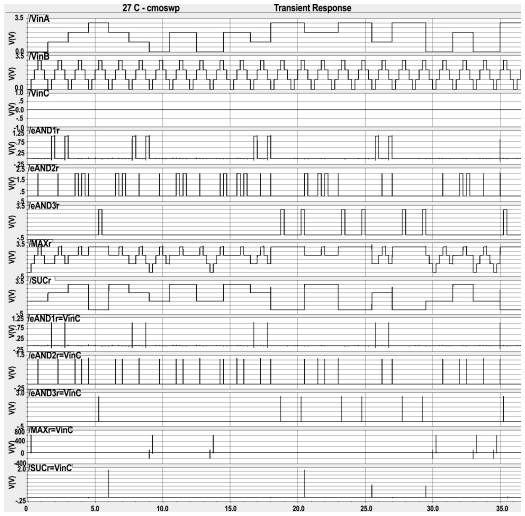

Fig. 10: Gates simulation 27°C cmoswp model

3 and N2 control switch (MP07, MP08) to set Sucessor1=2 level (when VinA=1, SUC_r=2); signal 2, N2 and N0 control switch (MN08, MN09, MP09) to set Sucessor1=1 level (when VinA=0, SUC_r=1); signal 0 controls switch (MN10) to set Sucessor1=0 level (when VinA=3, SUC_r=0). Table 11 shows the size of the CMOS transistors.

For implementation purposes of the quaternary gates to decrease circuit transistors counting it is better to implement specific circuits when Successor gates are needed in cascade instead of utilizing four, three or two SUC$_r$ gates in cascade, in which the only modification to build them is to set the correct output voltage in the original SUC$_r$ gate, this is not shown here.

4. RESULTS AND DISCUSSION

For illustration purposes, the forward and reverse computation for the $eAND_{ir}$, according to Figure 1, is shown in Figure 8. From top to bottom the correct results of the reversible gates VinA, VinB, VinC, the forward computation of $eAND_{ir}$, g0=VinA, g1=VinB (garbage), VinB=g$_{Br}$ (garbage), and the inverse computation of $eAND_{ir}$, that is $eAND_{ir}$=VinC (control signal), g0$_r$=g$_{Ar}$=VinA, g1$_r$=g$_{Br}$=VinB with the correct results are shown. Note that the input/output is a bijection, when the direct transformation is performed, the inputs are VinC=0, VinA, VinB and the outputs are $eAND_{ir}$, g$_{Br}$=VinB, g$_{Ar}$=VinA and for the inverse transformation $eAND_{ir}$=0, VinB=g$_{Br}$, VinA=g$_{Ar}$ recovering exactly the inputs.

Extensive simulations were performed for the tm,wp,ws models of the Cadence tool for 0°C, 27°C, 54°C and, for illustration purposes, Figure 9 shows the simulation for all the quaternary gates backward and forward computation for the tm model at 54°C and Figure 10 shows the simulation for all the quaternary gates backward and forward computation for the wp model at 27°C. The extensive simulations show that for all models up to 54°C all the simulations performs correctly.

The restriction for the ancillary input C=0 (only) suffices to implement the bijection in the restricted domain. Of course, it is possible to set VinC=1 or 2 or 3 to define other operator in the output, but it would increase a lot the circuit complexity without much more advantages due to the fact that, likely, each gate will be utilized to perform one operator only and if you include in one gate more operators, likely, it would be utilized only one operator and the others not, wasting a lot of operators in each gate. The implementation has the same drawbacks as the other implementation [30], as less noise rejection in comparison to the binary counterparts, increased number of transistor but less chip area, due to the fact that the interconnections are decreased which is about the 70% of the integrated circuit area.

5. CONCLUDING REMARKS AND FUTURE WORK

Reversible voltage mode quaternary gates have been implemented and verified by simulations in AMS CMOS 4ML C35B4E3 technology with results demonstrating correct functionality and feasibility of the electronic circuit. The objective is to decrease heat dissipation keeping constant the information entropy between the input and the output by means of reversible gates. Quaternary circuits have less noise rejection in comparison to the binary counterparts, increased number of transistor but less chip area. Simulations with Cadence models tm, wp, ws for temperatures: 0°C, 27°C, 54°C have shown correct functional behavior.

The universal quaternary set of gates already presented in the literature is implemented here with only 25, 18, 32, 10 and 32 CMOS transistors, respectively, outperforming past quaternary gates implementation for the non-reversible implementation by utilizing fewer CMOS transistors in more than 40%. Future works are related to further area reduction, computational performance and the IC nanometers manufacturing.

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