Abstract

The FPGAs will continue to be used for many of today’s challenging signal processing application. The reasons for this are firstly FPGAs are a form of highly configurable hardware, since it have reconfigurable gate structure which consumes more power.

The second reason is MIPS (Millions of instructions executed per second) and MMACS (Millions of Multiply-Accumulate Operations per Second) requirements of an application.

The main obstacle of using FPGA with processing of huge data is the limited number of pins of the FPGA kit that restrict the number of samples that must be processed simultaneously.

This paper describes an efficient FPGA based hardware design with the assistance of system generator applied for image processing and filtering algorithms. The used approach is a windowing operator technique to cut specified number of pixels from an image, and apply the filtering process to them. The median filter is used here, with two window sizes 3*3 and 5*5.
Xilinx software ISE 14.6 with (VHDL) language Spartan3-700A and MATLAB R2012a are the combined S/W for our application.

References

12. Xilinx System Generator user guide.

**Index Terms**

Computer Science  
Signal Processing

**Keywords**

FPGA, Xilinx system generator (XSG), Data processing, image processing.