Abstract

The FPGAs will continue to be used for many of today’s digital signal processing applications. The reasons for this are firstly FPGAs are highly configurable hardware, since it has a grid of reconfigurable gate structure. The second reason is MIPS and MMACS (Millions of instructions and Millions of Multiply-Accumulate Operations executed per Second) requirements of specific application. Although FPGAs have their limitations and processing restrictions. The main obstacle of using FPGA with huge data processing systems is the limited number of pins of the FPGA kit that restrict the number of input samples that must be processed simultaneously. This paper describes an efficient FPGA based hardware design with the assistance of XSG (Xilinx System Generator) applied for huge data systems. The used approach is a windowing technique to cut specified number of pixels from a huge data using Xilinx System Generator block sets to build the required digital system design that can be converted to a hardware
co-simulation design which is defined for FPGA environments. Image filtering techniques and algorithms are used in this work for testing the proposed approach. Xilinx software ISE 14.7 with (VHDL) language for Spartan3-700A and MATLAB R2013a are the combined S/W for hardware co-simulation design.

References

11. B. Draper, R. Beveridge, W. Böhm, C. Ross, M. Chawathe, "Implementing Image Applications on FPGAs", International Conference on Pattern Recognition, Quebec City, 2002.
12. Xilinx System Generator user guide.


**Index Terms**

Computer Science  
Signal Processing

**Keywords**

FPGA, Xilinx system generator (XSG), Data processing, image processing.