Delay Reduced 4 Bit Reversible Arithmetic Logic Units

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ABSTRACT

Power consumption is an important issue in today's world. Growing market of electronic system replaces the conventional digital system by reversible logic circuit to solve the problem of loss of information which was dissipated in the form of heat in irreversible circuit. As digital system implemented using AND and OR gates dissipates major amount of energy in the form of bit erased during logical operation where according to R. Landuer and Bennett concludes that one bit energy loss equalize the information loss in the form of KTln2 joules per bit per cycle unavoidable heat dissipation. Thus in this project, garbage free reversible computing system investigated from abstract design to physical gate level implementation. This proposed design is compared in terms of gate count, quantum cost and propagation delay. This reversible CPU designed using Feynman gate, Peres gate, Toffoli gate and DKG gate. It is synthesized on Xilinx 6.1i ISE and simulation result verifies the correction and modification of proposed design. Survey of this paper is based on types of reversible gates and four parameter that is gate count, ancilla input, garbage output, and quantum cost. This survey had great impact on quantum computing, nanotechnology, QCA, and low power VLSI.

Keywords
Reversible gates, Central Processing Unit (CPU), Garbage output, gate count, and quantum cost.

1. INTRODUCTION

Reversible logic device is one to one mapping and potentially recover and retain a fraction of the signal energy that can be reused by doing computation of forward path and undoing the computation by backward path. Reversible logic minimizes the garbage output and ancilla input by one to one mapping between input and output. It saves approximate 90% of energy dissipation by using the concept of Reversible Energy and Reversible Logic (RERL). This logic also helps in online and offline testing of faults.

Interest in reversible computation arises from the desire to reduce heat dissipation with higher densities and higher speed which cannot be possible with n inputs and one output as Rolf Landuer concludes that energy dissipates in the form of heat. One bit of energy equals to one bit of information loss which is KTln2 joules per bit per cycle. This energy loss is unavoidable

With n input one output which can be resolved by n input n output according to Charles Bennett. Thus reversible logic comes in the mind as Charles Bennett in 1973 concludes that under ideal physical circumstances with reversible logic, power dissipation is zero.

As design of reversible CPU is the toughest part to implement it practically. But advancement in VLSI design and portable device technologies lead to design faster, smaller and more compact system. Also due to multi-giga hertz processor and high end electronics increases the system complexity and high density packages. In order to avoid this physical limitation, researcher introduced reversible circuit as a promising alternative.

Zero energy dissipation is not possible practically under ideal physical circumstances due to lack of efficient tools and method for designing complex reversible circuit which can only possible if information lossless computation is performed. But an impressive progress has been made in the development of approaches for synthesis; implementation of reversible sequential element, and also in the development of hardware description language, employed to design complex system such as RISC CPU based on reversible gate. Then the state of the art design techniques becomes applicable to design large system and later on automatic synthesis approach becomes the major step towards the design of high end system in reversible logic which is applicable to function given in terms of truth table. Since the increasing demand of very low power VLSI and microelectronic device with negligible propagation delay to increase the speed of synthetization results the idea of above such research and progress on digital world. Thus reversible CPU based on reversible gates introduced.

2. REVERSIBLE PARAMETERS

Gate Count (GC): The number of gates used to realize the reversible circuit is known as gate count.

Ancilla Input (AI): The number of input kept constant at either 0 or 1 is known as ancilla input.

Garbage Output (GO): The number of unwanted or unused output of reversible gate is known as garbage output. It is needed to maintain reversibility. The input which regenerates at the output is not known as garbage output.

Quantum Cost (QC): The cost of the circuit in terms of cost of primitive gate is called quantum cost. It is a calculated by counting the number of V, V+, and CNOT gate.

3. BASICS OF REVERSIBLE GATE

Reversible gate is an n input and n output denoted by (n*n) circuit which produces a unique output pattern for each possible input pattern and it has one to one correspondence between the vector of inputs and output. This prevents the loss of information which is the root cause of irreversible logic circuit. It is used to designed an optimized circuit which is characterized as following

- Fan out and feedbacks or loops are not allowed.
- Garbage outputs, delay and quantum cost must be minimum.

3.1 Types of Reversible Gate

The simplest reversible logic gate is NOT gate and Controlled NOT gate (CNOT). Any reversible gate is realized by using 1*1 NOT gate and 2*2 reversible gates such as V (square root of NOT gate), V+ (hermitian of V) and Feynman gate (FG). The V and V+ quantum gates have following property

- V*V=NOT
- V*V+=V+*V=I
- V+*V+=NOT

Basic type of gates are explained as

NOT GATE

The reversible 1*1 gate is NOT gate with zero quantum cost. It is designed to produce the output states of P=A' where A is input of NOT gate. Their quantum implementations are shown in fig. 1.
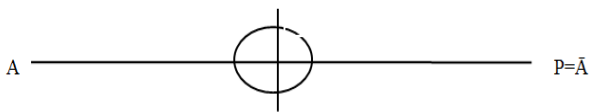
Figure 1: NOT gate quantum representation

FEYNMAN GATE

The controlled NOT gate of 2*2 reversible gate is known as Feynman gate. It is designed to produce following output states with inputs (A, B) is (P=A, $Q = A \oplus B$) . Its quantum cost and gate count is 1. Feynman gate is used to duplicate the signal when B=0. Feynman gate and its quantum representation is shown in figure 2 and figure 3 respectively
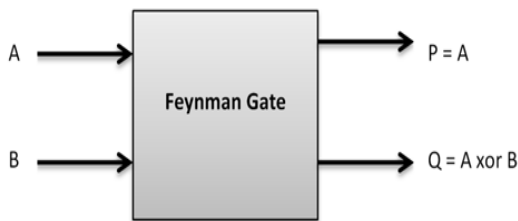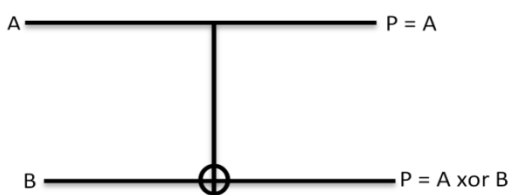

Figure 2: Feynman gate

Figure 3: Quantum representation of Feynman gate

FREDKIN GATE

It is 3*3 reversible gate and designed to produce the following output states with inputs (A, B, C) is (P=A, $Q = A^1 B \oplus AC$ $R = A^1 C \oplus AB$). Quantum cost and gate count of this gate is 5 and 6. Fredkin gate and its implementation are shown in figure 4 and figure 5 respectively
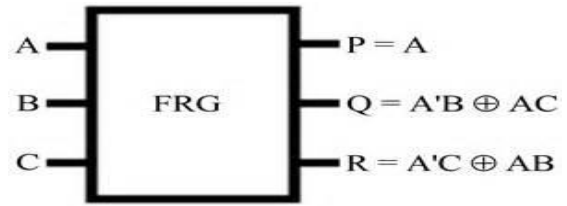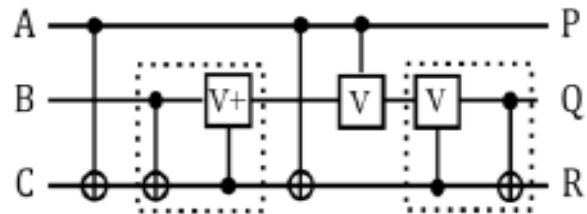

Figure 4: Fredkin gate

Figure 5: Quantum representation of Fredkin gate

PERES GATE

It is 3*3 reversible gates, designed to produce the following output states with inputs (A, B, C) is ($P = A \quad Q = A \oplus B$ $R = A.B \oplus C$). Quantum cost and gate count of this gate is 4 and 3. Peres gate and its implementation are shown in fig 6
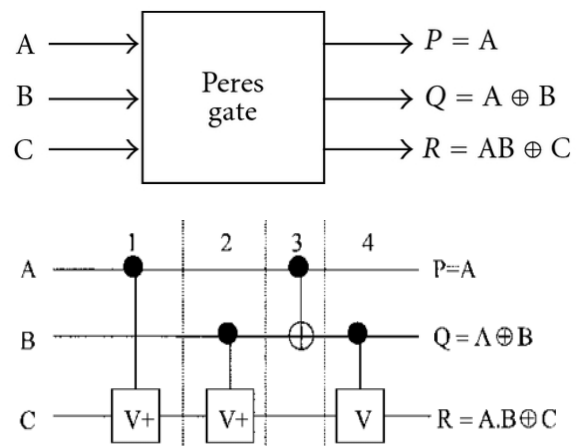

Figure 6: Peres gate and its quantum circuit implementation

TOFFOLI GATE

It is 3*3 reversible gate, designed to produce following output states with inputs (A, B, C) is (P=A Q=B $R = A.B \oplus C$). Quantum cost and gate count of this gate is 5 and 2. Toffoli gate and its implementation are shown in figure 7 and 8 respectively
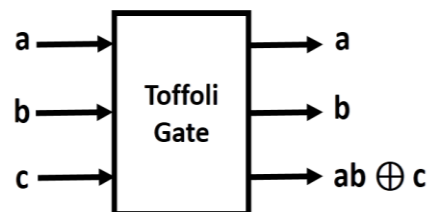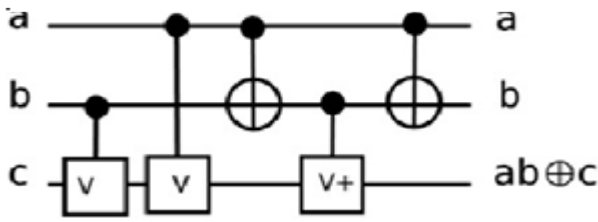

Figure 7: Toffoli gate

Figure 8: Quantum representation of Toffoli gate

DKG GATE

It is 4*4 reversible gate, designed to produce the following output states with inputs (A, B, C) is ($P = A$, $Q = B$ $R = A'C + AD$ $S = (B \oplus C \oplus D)$). It works as reversible full adder when A=0 and works as reversible full subs tractor when A=1. Thus it requires at least two garbage output to make output combination unique. Quantum cost and gate count of this gate is 10 and 6. DKG gate and its quantum representation is shown below in figure 9 and figure 10 respectively
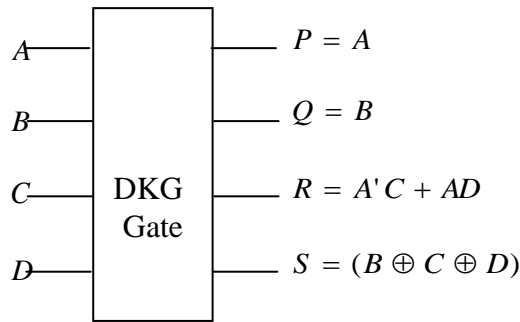

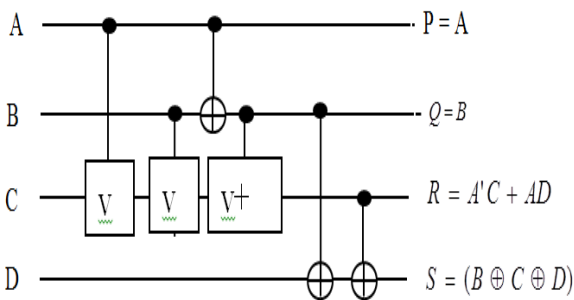**Figure 9: Block diagram of DKG gate**

Figure 10: Quantum circuit implementation of DKG gate

4. SIMULATION RESULT

More specifically, we have developed new garbage-free circuits for addition and are working towards a general multiplication circuit. We have also combined multiple operations together to implement a reversible arithmetic logic unit. With these and other garbage-free arithmetic circuits it is possible to design larger reversible computing systems. As an example, we have implemented discrete lossless transforms by redesigning these with a lifting scheme. We have also shown the design of a reversible computing architecture and implemented this using only reversible logic gates. While, these are still small systems, with further development it

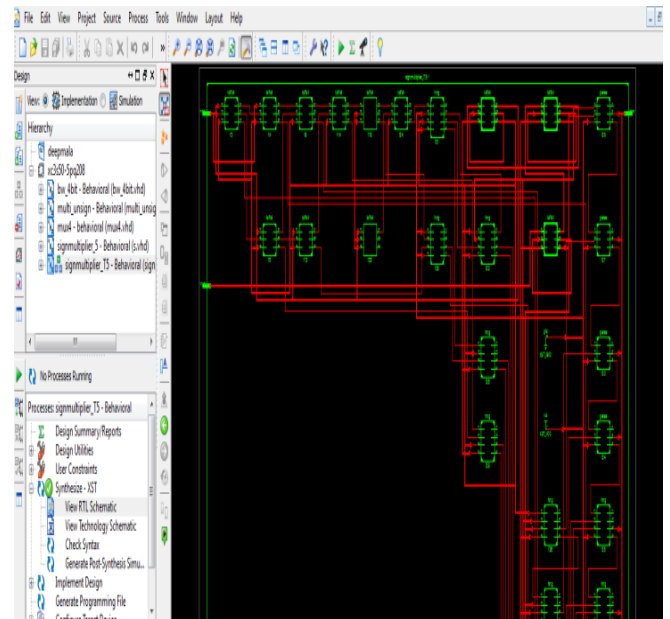should be possible to use similar strategies to implement even larger systems.

Figure 11: Register transfer level (RTL) using signed 4-bit multiplication

From our own design experience, we know that designing logic gate-level circuits quickly becomes complicated when the functionality and number of wires involved are increased. To make the design process easier, we have developed two hardware description languages. Using examples from known reversible circuits, we have shown that circuits can be described reasonably concisely. These are, however, still small examples and we need to implement a larger system to show the usefulness of the languages.

Table 1: Syntheses Result for Reversible 4-bit, 8-bit, 16-bit and 32-bit Adder/Sub tractor with different Device Family

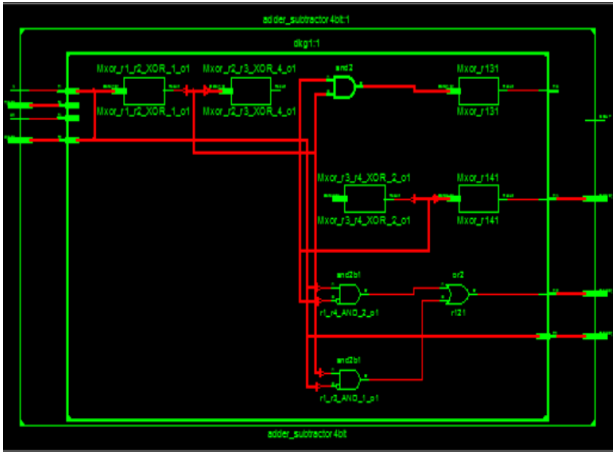| Device Family	Adder/ Sub-tractor	Number of Slice	4 Input LUTs	Maximum Combination Path Delay
Spartan-3	4-bit	7	12	12.50ns
	8-bit	14	25	18.89 ns
	16-bit	28	50	31.68 ns
	32-bit	57	100	56.54 ns
Sparten-3E	4-bit	7	12	9.60 ns
	8-bit	14	25	14.72 ns
	16-bit	28	50	24.64 ns
	32-bit	57	100	44.13 ns
Spartan-6	4-bit	7	12	7.02 ns
	8-bit	14	25	9.55 ns
	16-bit	28	50	14.50 ns
	32-bit	57	100	24.17 ns

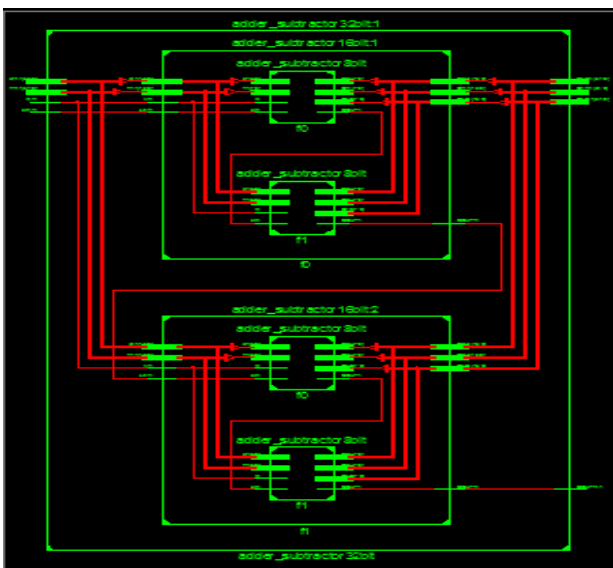**Figure 12: RTL view of 4-bit Adder/Sub tractor**

Figure 13: RTL view of 32-bit Adder/Sub tractor
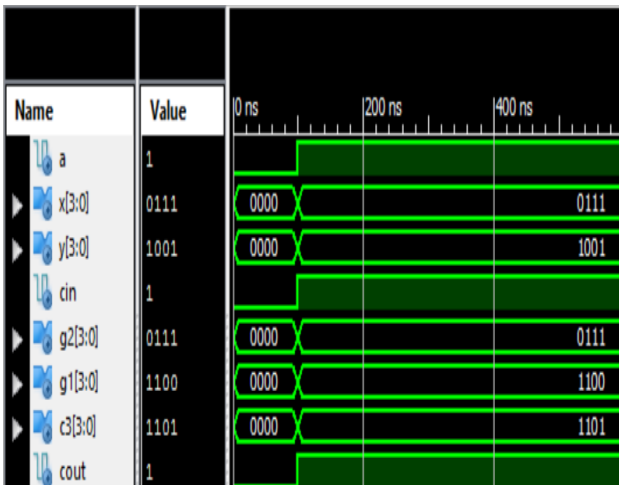

Figure 14: Output waveform of the 4-bit Adder/ Sub-tractor Circuit

Table II: Comparative Results of Existing Algorithm and Proposed Algorithm in 4-bit

Parameter	4-bit Reversible Full Adder [1]	Reversible FA using Peres Gate	4-bit Reversible Full Sub tractor [1]	Reversible FS using TR Gate
AI	12	4	12	4
GO	8	8	8	8
QC	72	32	80	48
Delay	66	48	66	40
GC	24	20	32	28
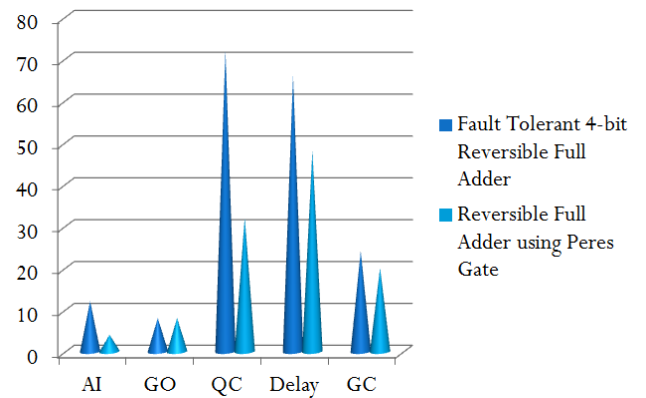
Figure 15: Bar Graph of the Previous and Proposed Reversible Full Adder

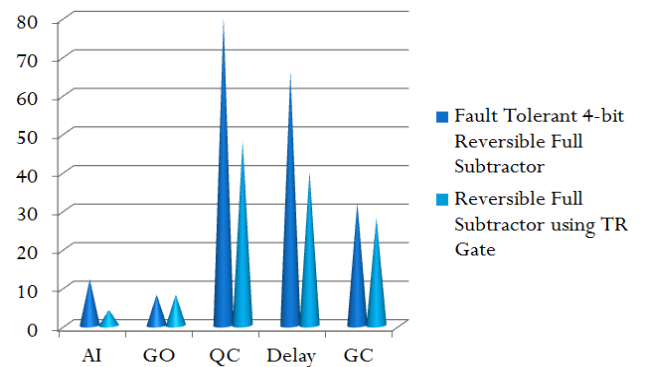**Figure 16: Bar Graph of the Previous and Proposed Reversible Full Adder**

Table III: Comparative Results of Existing Algorithm and Proposed Algorithm in n-bit

parameter	Reversible 5-bit Sign Multiplier using DKG Gate	Reversible n-bit Sign Multiplier using DKG Gate
AI	45	9n
GO	41	8n+1
QC	237	47n+2
Delay	74	14n+4
GC	222	44n+2

5. CONCLUSION

For conventional logic circuits there exists much research, even whole books, dedicated to the design and implementation of computer arithmetic. This is definitely not the case for reversible logic. The constraint is that, the circuits must be garbage-free is what makes it an interesting research problem, but most proposed designs (both hand-made and CAD generated) still implement the conventional algorithms with garbage. This research works on reducing delay with reduced garbage from existing RALU which in result increases the speed and improves the performances of overall architecture of the computer arithmetic.

In near future components can be designed to further reduce the design parameter in a way the established circuit increase the speed and reduce the cost of the circuit. A numerous number of other gates can be designed using search methods to further improve the performance with low power. Design can be extended to n bit for ALU and executive methods may be used to find the reversible gates with an optimal solution with simulating result for area and power.

6. REFERENCES

[1] Jayashree H V and Ashwin S, "Berger Check and Fault Tolerant Reversible Arithmetic Component Design", Internatioanal Conference of Digital Signal Processing and Circuit System, PP. 656-659, IEEE 2015.

[2] Lafifa Jamal and Hafiz Md. Hasan Babu, "Design and Implementation of a Reversible Central Processing Unit", IEEE Computer Society Annual Symposium on VLSI, Vol. 45, Issure 07, IEEE 2015.

[3] Hatkar A. P., Hatkar A. A. and Narkhede N. P., "ASIC Design of Reversible Multiplier Circuit", International Conference on Electronic Systems, Signal Processing and Computing Technologies, PP. 01-07, IEEE 2014.

[4] Morrison and Nagarajan Ranganathan, "Design of a Reversible ALU based on Novel Programmable Reversible Logic Gate Structures", Computer Society Annual Symposium on VLSI, PP. 456-461, IEEE 2013.

[5] Mr. Abhishek Gupta, Mr. UtsavMalviya and Prof. VinodKapse, "Design of Speed, Energy and Power Efficient Reversible Logic Based Vedic ALU for Digital Processors", Computer Society Annual Symposium on VLSI, PP. 01-05, IEEE 2012.

[6] Akanksha Dixit and Vinod Kapse, "Arithmetic & Logic Unit (ALU) Design using Reversible Control Unit", International Journal of Engineering and Innovative Technology (IJEIT) Volume 1, Issue 6, June 2012.

[7] LekshmiViswanath and Ponni.M, "Design and Analysis of 16 Bit Reversible ALU", Volume 1, Issue 1, PP 46-53, June 2012.

[8] M. Morrison and N. Ranganathan, "Design of a Reversible ALU Based on Novel Programmable Reversible Logic Gate Structures," IEEE International Symposium on VLSI, PP. 126-131, IEEE 2011.

[9] Md. Belayet Ali, Hosna Ara Rahman and Md. Mizanur Rahman, "Design of a High Performance Reversible Multiplier", IJCSI International Journal of Computer Science Issues, Vol. 8, Issue 6, No 1, November 2011.

[10] Indrayani Patle, Akansha Bhargav and Prashant Wanjari, "Implementation of Baugh-Wooley Multiplier Based on Soft-CoreProcessor", IOSR Journal of Engineering (IOSRJEN), Vol. 23, Issue 05, May 2010.

[11] Indrayani Patle, Akansha Bhargav and Prashant Wanjari, "Implementation of Baugh-Wooley Multiplier Based on Soft-CoreProcessor", IOSR Journal of Engineering (IOSRJEN), Vol. 23, Issue 05, May 2010

[12] H. Thapliyal and N. Ranganathan, "Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage Outputs,"ACM Journal on Emerging Technologies in Computing Systems, Vol. 12, Issue 4, April 2010.

[13] H. Thapliyal and N. Ranganathan, "Reversible Logic Based Concurrently Testable Latches for Molecular QCA," IEEE Transactions on Nanotechnology, Vol. 9, Issue. 1, PP. 62-69, IEEE 2010.

[14] M. Nachtigal, H. Thapliyal, and N. Ranganathan, "Design of a Reversible Single Precision Floating Point Multiplier Based on Operand Decomposition," To appear in Proc. of 10th IEEE International Conference on Nanotechnology , PP. 01-06, IEEE 2010.

[15] M. K. Thomson, Robert Gluck and Holger Bock Axelsen, "Reversible Arithmetic Logic Unit for Quantum arithmetic", Journal of Physics A: Mathematical and Theoretical. Volume 43, Issue 04, April 2010.

[16] N. Nayeem, A. Hossain, M. Haque, L. Jamal, and H. Babu, "Novel reversible division hardware," in Circuits and Systems, MWSCAS '09. 52nd IEEE International Midwest Symposium on, 2009, pp. 1134 −1138, IEEE 2009.

[17] H. Axelsen, R. Glck, and T. Yokoyama, "Reversible machine code and its abstract processor architecture," in Computer Science Theory and Applications, ser. Lecture Notes in Computer Science. Springer Berlin Heidelberg, Vol. 46, Issue 4, PP. 56–69, 2007.

[18] H. Thapliyal, M.B. Srinivas, "Novel design and reversible logic synthesis of multiplexer based full adder and multipliers", 48th IEEE MIDWEST Symposium on Circuits and Systems (MWSCAS 2005), Cincinnati, Ohio, USA, PP.1593-1596, August 7–10, 2005.

[19] M. Khan, "Design of Full-Adder with Reversible Gates," Proceedings of 5th International Conference on Computer and Information Technology, PP. 515-519, IEEE 2002.

[20] D. P. DiVincenzo, "Quantum gates and circuits," Proceedings of the Royal Society of London A: Mathematical, Physical and Engineering Sciences, vol. 454, no. 1969, pp. 261–276, 1998.

[21] C. H. Bennett, "Logical reversibility of computation," IBM J. Research and Development, vol. 17, pp. 525–532, 1973.

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