SRAM based Fault Tolerant Technique for Detection of Transient Errors in Processors through Pass Transistor Logic

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Authors:
S. Ravi Chand, T. Madhu, M. Sailaja

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Abstract

In digital domain applications SRAM-based FPGAs are increasingly becoming more popular and the most essential analyses is to verify the performance of the system whether fault occurred. The error models of SRAM-based due to SEUs are more complicated. The cell library and synthesis tools are developed based on pass-transistor, to clarify the potential of top-down pass-transistor logic. The paper focus on fault tolerant technique implied on software, an extensive approach for Static Random Access Memory SRAM block in multi core architectures using ‘n’ transistor technique. The SRAM circuit is tested for its functionality. The n transistor techniques use a software-centric approach transient fault tolerance, which makes certain for perfect execution of software. In this approach the applied methodology for SRAM accessible in the processor. Presented our fault tolerance techniques for detection of transient errors in the processors. Implementing this combination has resulted in 100% fault detection for the techniques applied various applications. Comparative results display a distinguished advantage of the proposed technique which could be combined with data flow techniques, and can have high detection ratios for real applications.
References

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Index Terms

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Keywords

SRAM, Fault Tolerance, Process Level Redundancy, Pass Transistor Logic.