SRAM based Fault Tolerant Technique for Detection of Transient Errors in Processors through Pass Transistor Logic

S. Ravi Chand
Research Scholar, JNTUK, Kakinada, Andhra Pradesh,

T. Madhu
Professor in ECE, Swarnandhra Inst. of Engg. and Tech., Narasapur, Andhra Pradesh, India

M. Sailaja
Professor in ECE, JNTUK, Kakinada, Andhra Pradesh, India.

ABSTRACT
In digital domain applications SRAM-based FPGAs are increasingly becoming more popular and the most essential analyses is to verify the performance of the system whether fault occurred. The error models of SRAM-based due to SEUs are more complicated. The cell library and synthesis tools are developed based on pass-transistor, to clarify the potential of top-down pass-transistor logic. The paper focus on fault tolerant technique implied on software , an extensive approach for Static Random Access Memory SRAM block in multi core architectures using 'n' transistor technique. The SRAM circuit is tested for its functionality. The n transistor techniques use a software-centric approach transient fault tolerance, which makes certain for perfect execution of software. In this approach the applied methodology for SRAM accessible in the processor. Presented our fault tolerance techniques for detection of transient errors in the processors. Implementing this combination has resulted in 100% fault detection for the techniques applied various applications. Comparative results display a distinguished advantage of the proposed technique which could be combined with data flow techniques, and can have high detection ratios for real applications.

Keywords
SRAM, Fault Tolerance, Process Level Redundancy, Pass Transistor Logic.

1. INTRODUCTION
Transient faults, also called as soft errors, which distress about the reliability in a computer systems [1]. Transient fault occurs even in the presence of error. Fault cause error results failure. Fault cause error observed by deviation from expected behavior results failure. The event of occurrence (e.g., cosmic particle strikes, power supply noise, device coupling) alleviation or exclusion of sufficient charge to invert the state of transistor. The inverted value may cause the effect in program execution. Current trend in process technology shows that the future error rate will remain comparatively constant [2]. The number of usable transistor per chip continuously grows in an exponential manner, which increases dramatically. These trends had shown that to ensure correct execution operation of systems. Transient fault characteristics are reliability, dependability, accessibility and availability. The memory is easily protected with error correcting code and parity within high performance microprocessor [3]. However, the identically specified techniques could not be adopted directly for general purpose computing domain.

Application specific constraints fault results in glitch generation, which may be unnoticed by the user. At these instances the reliability improves to congregate user prospect of failure rates. While software technique cannot render a reliability level of hardware technique, they significantly provides a low cost and flexible (zero hardware design cost).existing software transient fault tolerance approaches use the encyclopedias to insert redundant instructions for checking computation and control flow process. Redundant more than is needed, desired or required to ensure correct execution [4].

2. DESIGN AND SIMULATION OF A 10T SRAM CELL
Design of 10T SRAM is designed as 8T SRAM, a couple of transistors are coupled to read decoupled path using bit lines (BL & BLB) preventing the drain of read current to ground. The design structure of 10T cell is similar to particular ended 8T cell; two transistors are included to 8 transistor design at read decoupled path.

SRAM reveal data reminisce, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered. Static memory which is mainly used for a storage device it is a permanent storage. Shift register which are essential modules of sequential logic circuit mostly used for storing bits. They are group of flip-flops coupled in a chain. The output of first flip-flop becomes the input of second flip-flop and so on. All flip-flops applied by a common clock pulse which performs set or reset concurrently. Two redundant processes , out of which one is labeled master process and the second as slave processes. Here we used a adder application here two half adder as designed as a full adder which propagates the sum and carry output.

Optimizing area, power and delay in SRAM needs for optimized design. To characterize the behavior of memory, SRAM in particular, modeling of memory has become essential which helps in taking critical decisions of design issues before simulating on Spice. Many models were proposed and tools were developed to assess the performance of SRAM in past years based on traditional 6T, 6.5T, 8T and 10T SRAM design.

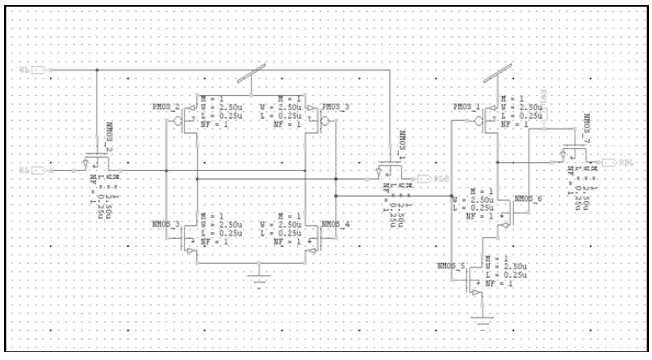

Fig.1. Design of a 10T SRAM cell

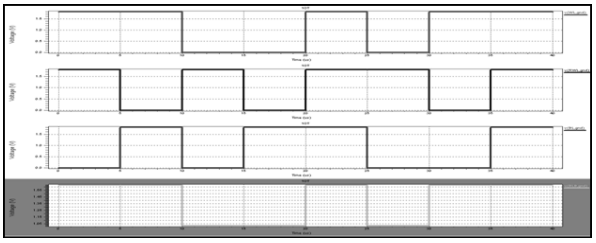

Fig .2.Measured Waveform for 10T SRAM

Here to design the PLR circuit for transient fault design. This circuit consists of four stages1) Memory block 2) shift register 3) master and slave process 4) watch dog timer

The schematic digram of basefull circuit using 10T SRAM

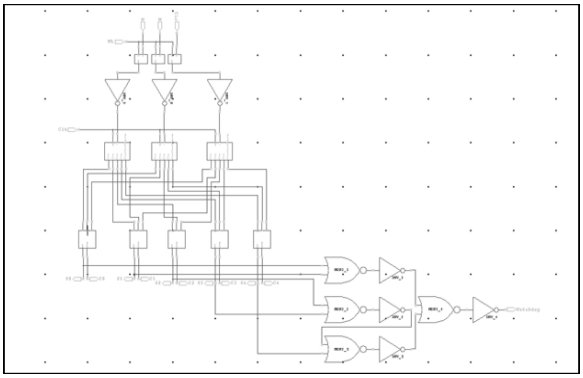

Fig.3.Structure Of 10T SRAM Based Base Full Schematic

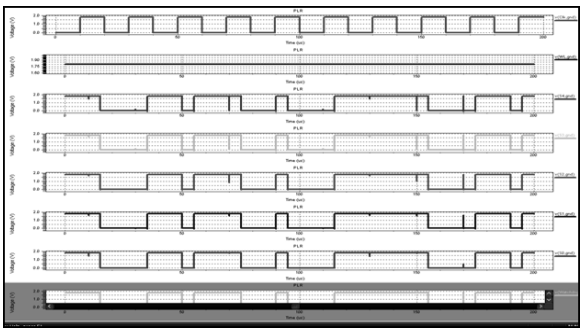

Fig..4.Simulated Output For Fault Free Output

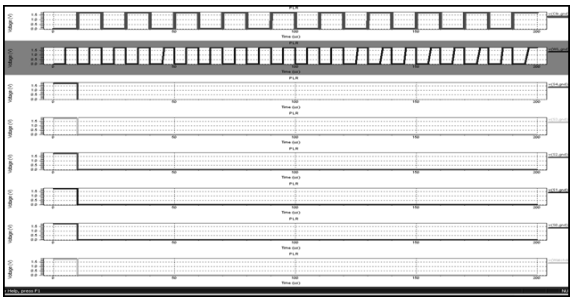

Fig.5.Simulated Output For Faulty Output

3. PASS TRANSITOR LOGIC

A periodic clock signal drives a pass transistor to act as a switch, both for charge up or discharge down the unwanted capacitance. Thus, the switching operations performed when clock signal is active (ck=1) are the logic "1" transfer and the logic "0" charging down the low level in any case ,the output of the depletion load NMOS invertor assumes a logic low or a logic high depending on levels of voltage. The architecture of a 10T SRAM cell is similar to the PTL cell except additional read circuitry 2 shows the designed 10T SRAM cell. In this 10T SRAM cell, 10 transistors have been used. Dual-pass transistor logic completely removes a few inverter stages essential for CPTL by utilizing a combination of NMOS and PMOS transistors, with double logical paths for specific function. Even though the process is high speed planned for at a certain time at less capacitance at the input, it has inadequate voltage capacity to drive a load. The DPL gate consisting CMOS is being switched, in contrast with switching tree of a CPL gate, by using NMOS transistors only. By adding PMOS transistors in shunt with the NMOS transistors Full swing operation is attained. Increase in input capacitance is obtained by this addition. The switching tree of a CPL gate consists of NMOS transistors, resulting lower input capacitance. The full- voltage output swing restoration of a DPL-gate is accomplished by the combination of an N and PMOS transistor, instead of the PMOS-latches and inverters which are performed by Complementary Pass Transistor logic (CPTL). Dual pass-transistor logic (DPL) assumes both PMOS and NMOS transistors of PTL network to keep away from incomplete swing problems, and reflects in elevated area and power limitations

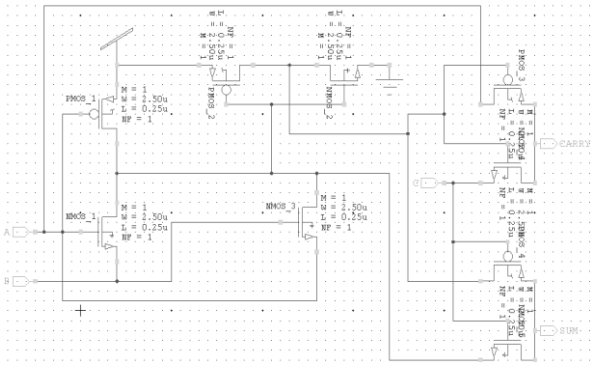

Fig.6. Pass Transistor Logic

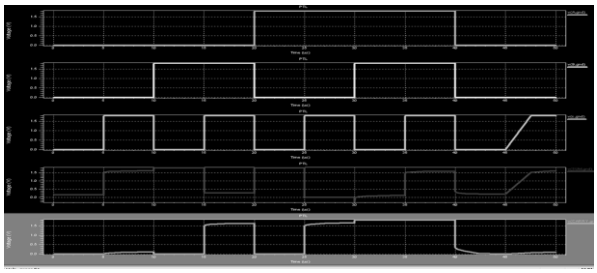

Fig.7 waveform for PTL Logic

4. ASS TRANSISTOR LOGIC USING BASE FULL SCHEMATIC

The schematic design figure shown below with three redundant processes. Thus, the reliability improves to meet user expectations of failure rates. This is mainly used to leverage overhead mechanism.

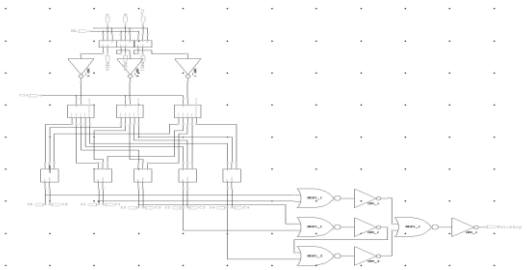

Fig.8: Base Full Schematic Using PTL

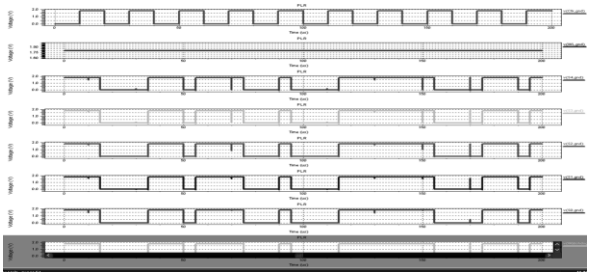

Fig.9: Fault free output

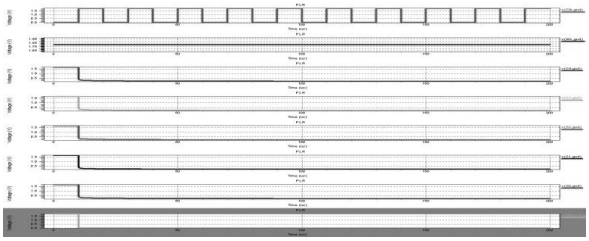

Fig.10: Faulty output

Compared to 10T SRAM basefull and 10T SRAM basefull schematic using PTL has numerous advantages switching activity get reduced and both power & delay get decreases.

5. POWER ANALYSIS AND OPTIMIZATION EXPERIMENTAL RESULTS

To optimize the average power, static power ,static current, energy delay product, operating frequency, area of transistor, throughput.

The two major issues to be considered in VLSI design and synthesis are power and delay which rely on various parameters of design metrics. Considering channel length power consumption and delay are assumed for base full schematic design. Using tanner EDA tools (T-Spice) simulation results are obtained for various circuits.

The delay and power dissipation engaged for changes in supply voltages will differ with techniques applied, by decreasing power supply voltage dissipation of power also decreases (P_d α $\sqrt{V_{dd}}$) and propagation delay (t_p) reflects inverse proportionality to power supply.

This power result we calculate

Power Delay Product [(PDP = average power consumed * propagation time delay), in fJ (10^-15)]

Static current I=P/V (mA)
Operating frequency=1/T HZ
$=1/T_{On}+T_{Off}$

To calculate the Area of Transistor:

Area of transistor=No. of transistor*length * width (um^2)

Throughput = operating frequency*No. of bits at output (bits/sec)

SRAM is semiconductor memory cell. It stores one bit of information. It is faster and consumes very less power as compared to other memory cells. SRAM is vital component in a chip or microprocessor IC. 10T SRAM cell performs better than 6T.

The following comparison table 1 shows that the detail about the design of 10T.In those table four parameter has been explained with fault injection

TABLE 1 Comparison Study For 10T

Parameters	10T	10T Base full	PTL	PTL Base full
Injected Faults	1089	11249	11355	24589
Power average	4.3µw	109µw	1.4µw	17.2µw
Static power	11µw	8.63mw	1.2mw	1.55mw
Static current	6.1µA	4.7mA	0.6mA	0.86mA
Energy Delay Product	57.90nws	604.5nws	57.90nws	0.6104nws
Operating frequency	25Hz	25Hz	25Hz	25Hz
Area of transistor	$6.25um^2$	$6.25um^2$	$5um^2$	$5um^2$
Throughput	25bits/sec	25bits/sec	25bits/sec	25 bits/sec

The optimization is based on the simulation results of 10T of average power consumed power and delay we calculate the following table from this we optimize the how power consumed and concluded that the 10 T SRAM using the application pass transistor logic has advantageous compared to 10T SRAM.

Table .2 Comparative Study Of Power & Delay For Base Full Schematic

Parameters	SYSTEM with nT	SYSTEM with PTL logic
Injected Faults	11249	24589
Power average	0.109mw	0.0172mw
Static power	8.63mw	0.155mw
Static current	4.7mA	0.086mA
Energy Delay Product	604.5nws	2.332nws
Operating frequency	25Hz	25Hz
Area of transistor	$6.25um^2$	$5.625um^2$
Throughput	25 bits/sec	25bits/sec

The base full schematic consists of two blocks that is memory block, shift register, master and slave process and watch dog timer. The total base full schematic consumed the average power, static power, static current, energy delay product be optimized table 2 shows that the four parameters comparative study for 10T.

Table .3 Comparative study of Power Delay Product

Design	Power	Delay	Power delay product
10T CELL	$1.148*10^{-005}$	$1.700*10^{-006}$	$5.7905*10^{-11}$ws
P T L	$1.222*10^{-003}$	$1.000*10^{-005}$	$1.222*10^{-8}$ws
10T base full	$8.637*10^{-003}$	$7.000*10^{-006}$	$60.459*10^{-8}$ws
10T using PTL	$1.555*10^{-002}$	$1.500*10^{003}$	$2.3325*10^{1}$ws

SRAM is vital component in a chip or microprocessor IC. 10T SRAM cell performs better then 10T SRAM cell using PTL in terms of reliability and stability. PTL cell has less reliability at low supply voltage due to degradation in noise margins. Power dissipation, delay and power delay product of the designed base full 10T SRAM, & 10T SRAM cell using PTL.

The architecture of a 10T SRAM cell is similar to the 6T SRAM cell except additional read circuitry 2 shows the designed 10T SRAM cell. In this 10T SRAM cell, 10

transistors have been used. It consists of conventional 6TSRAM cell and an additional read circuitry. Difficulty in conventional 6.5T SRAM cell is the high risk of data loss during read operations. There is possibility of flipping node voltage at Q and Q' due to back to back inverter actions. This situation can be avoided using extra read circuitry. In this 10T SRAM cell, write operation is same as in 6T SRAM cell .In case of read operation, charge sharing takes place between read bit line (RBL) and uncharged bit line BL / BLB during read operation. Compared to 6T SRAM, 6.5T SRAM and 8T SRAM, 10T SRAM has numerous advantages switching activity get reduced and both power & delay get decreases

6. CONCLUSION & FUTURE WORK

This has motivated software fault tolerance in transient faults which necessitates for general purpose processors and proposed Process Level Redundancy as sense of appealing as a substitute in prominent multi core processors. Idleness at the process level is a provision; PLR takes maximum advantage to schedule freely applicable processes to every hardware modules in the available resources. PLR can be deployed without any alterations to the existing application, Operating Systems, hardware in the system. PLR sustaining single-tasked applications is presented and assessed for coverage of faults and performance. As a proof Fault injection experimented upon software-centric fault detection model of that PLR's which has higher efficiency in detecting faults and safely benign faults are neglected. Present a software implemented transient fault tolerance technique to utilize general purpose hardware with multi cores. PLR performance meliorates on presented software transient fault tolerance techniques and moves towards enabling software based fault tolerant solutions almost equivalent performance against hardware techniques.

Performance metrics to be considered for SRAM design are: stability, power, delay and area. Which are expressed in terms of sizing. Assumed a better design with high stability as basis for comparison. As Vdd scales down the delay, power, and EOP of every design are put for comparison. The obtained EOP for 10T design is very minute and proved as efficient in terms of area and low EOP region.

Thus, it can be concluded that focuses on a method of charge sharing between the bit lines of 10T SRAM and these method consumes less power for read operations and cut systems dynamic power budget to greater extent as compare to 8T SRAM & 6T SRAM. Power consumption of 10T SRAM gets reduced by a factor when compared to its counterpart 8T 6 T SRAM Cell. The significant improvements obtained in the results through the use of 10T cell which will be applicable for future low power memory design. Applications such as sensor network domain that is battery driven application. Finally concluded power reduction at 10 T SRAM both power and delay get decreases and also switching activity is reduced.

To Remove all glitch in the circuit and to design a fault free circuit. In future work, we will design a processing unit circuit and study about how to design circuits with multiple outputs. Show comparison of power consumption. Future work involve exploring parameters for energetically adapting the level of redundancy, To make certain determination in many more complex applications which are inclusive of shared memory, signals, interrupts, and multi threading. Are can be discovered by the current method.

Presented our technique for fault tolerance to analyze and detect transient errors in Multi core processors. As a result a collective result in 100% fault detection for each technique applied to all case study applications. Such results prove that the proposed technique could be united with data flow techniques, Voltage level at logic levels, to obtain high detection rates for real time applications.

7. REFERENCES

[1] Alex Shye, Student Member, IEEE, Joseph Blomstedt(.2013), 'PLR: A Software Approach to Transient Fault Tolerance for Multi core Architectures' IEEE transaction on dependable and secure computing.

[2] Alex Shye Tipp Moseley† Vijay Janapa Reddi Joseph Blomstedt Daniel A. Connors (2013), 'Using Process-Level Redundancy to Exploit Multiple Cores for Transient Fault Tolerance' IEEE transaction on dependable and secure computing.

[3] Christopher Weaver1, Joel Emer1, Shubhendu S. Mukherjee1, and Steven K. Reinhardt1, 2(Jan.2007),'Techniques to Reduce the Soft Error Rate of a High Performance Microprocessor', Proc. Ninth Int'l Conf. Architectural Support for Programming Languages

[4] Graham E. Fagg, Edgar Gabriel, Zizhong Chen, Thara Angskun, George Basilica, Jelena, and Jack J. Dongarra(Feb. 2011), 'Process Fault-Tolerance: Semantics, Design and Applications for High Performance Computing

[5] Hamid Mushtaq, Zaid Al-Ars, Koen Bertels(DSN '10),'Efficient Software-Based Fault Tolerance Approach on Multi core Platforms' Proc. 37th Int'l Conf. Dependable Systems and Networks).

[6] Iwagaki, T; Nakaso, T Ohkubo, R; Ichihara, H (Feb. 2009.), 'scheduling algorithm in data path synthesis for long duration transient fault tolerance', IEEE Reliability Physics Tutorial Notes, Reliability Fundamentals, pp. 121_01.1-121_01.14.

[7] Karthik, Sundaramoorthy, Zach Purser Eric Rotenberg (July .2008), 'slipstream processors: improving both performance and fault tolerance', in Proc. Ninth Int'l Conf. Architectural Support for Programming Languages and Operating Systems (ASPLOS)

[8] Lau Cheuk Lung1, Fabio Favarim2, Giuliani Teixeira Santos1, Miguel Correia3 (Sep .2004.), 'An Infrastructure for Adaptive Fault Tolerance on FT-CORBA '.

[9] Naiouf and Armando De Giusti1, 3 has analyzed (Feb. 2010) 'A tool for detecting transient faults in execution of parallel scientific applications on multi core clusters', IEEE transaction on defect and fault tolerance in VLSI technology volume.