Abstract

One of the main detection duties in spectroscopy system is pileup detection of the location of the maximum peaks utilizing a local extreme method. This paper presents the hardware implementation of two pile up recovery algorithms. The first algorithm utilizes a peak detection algorithm, while the second one utilizes a peak sensitivity algorithm. The two algorithms are designed and evaluated by compiling MATLAB into field programmable gate array (FPGA) using Xilinx system generator (XSG). The tested signal is captured by analogue to-digital converter (ADC) with sampling rate of 16MS/s. The results confirm that the first algorithm is better than the second one due to its simple architecture, which leads to faster processing speed.
Hardware Implementation for Pileup Correction Algorithms in Gamma Ray Spectroscopy

References


Index Terms

Computer Science

Algorithms
Keywords

Pulse pile up, Digital signal processing, XSG, FPGA