# Switching Frequency Selection Technique for Model Predictive Control based Multilevel Inverter

Md. Tariquzzaman Department of EEE, Jashore University of Science and Technology Md. Tanvir Ahammed Department of EEE, Jashore University of Science and Technology Md. Moznuzzaman Department of EEE, Jashore University of Science and Technology

# ABSTRACT

Selection of proper switching frequency of an inverter is very dominant factor for system reliability and performance. Model predictive control (MPC) strategy selects optimal switching state in every sampling instant for the inverter by diminishing cost function. As a result, MPC based multilevel inverter requires higher sampling frequency in comparison with pulse width modulation (PWM) which incurs higher switching frequency. So, optimal selection of switching frequency is required for enhancing system reliability and performance. This paper presents an optimum switching frequency technique for three-level neutral-point clamped (3L-NPC) inverter. The cost function of MPC based 3L-NPC inverter has three control objectives namely current tracking error, neutral point voltage balancing and, the number of switching transitions are included in the cost function with weighting factor. The value of the weighting factor in the cost function is selected by making a trade-off among the current total harmonic distortion (THD), neutral voltage balancing and, the average switching frequency. To evaluate the system performance switching loss is determined at the optimal switching frequency as well as without the switching frequency optimization.

## **General Terms**

Model predictive control, Neutral point clamped.

# Keywords

Model predictive control, neutral point clamped, switching loss, neutral point voltage balancing, current total harmonic distortion (THD).

# 1. INTRODUCTION

Inverters, also known as dc to ac controller, are basically electronic devices which converters a dc signals into ac signals. Based on different circuit configurations, inverters can produce square waveforms, modified square waveforms, modified sine waveforms etc. Recently, multilevel inverters become a popular choice in comparison with conventional two level inverter for integrating smart grid, ac motor drives applications, reactive power compensation and so on [1]. Multilevel converters possess some attractive features namely low total harmonic distortion of the inverter output current waveforms, a suppression in switching stress, a reduction in switching loss, higher voltage operation of the inverter, and required smaller size of interfacing transformers and output filter arrangements [1]-[6].

Different types of multilevel inverter (MLI) topologies are available such as cascaded H-bridge (CHB) inverter topologies required a costly and larger transformer for providing isolated dc sources [2], [3], [6], flying capacitor (FC), neutral point clamped (NPC) or diode clamped inverter. Among them, one of the mostly used single-DC-Source MLI topologies is the 3-level NPC [7] but this topology suffers with neutral point voltage balancing (NPVB) problem. Again, higher switching frequencies are required for balancing capacitor voltages of FC topology which in a sense increase the power loss of the system. So, reduction of switching frequency is an important issue. To mitigate this problem, different types of methods have been adopted in the literature [8]-[9]. In this research work, NPC has been used as a multilevel inverter.

The control scheme of the MLIs plays an important role to guarantee system stability and enhance efficiency. Different control schemes are available such as pulse width modulation (PWM), space vector pulse width modulation (SVPWM) control, selective harmonic elimination PWM (SHE-PWM), model predictive control (MPC) etc. Among them, MPC has drawn significant attention to the power electronic community due to the advancement of microprocessor. MPC has the feature of designing controller of having multiple constraints. It minimizes the cost function carrying number of constraints and gives optimum solution at every sample time instant. There are two types of MPC: finite-state MPC (FS-MPC) and continuous control set MPC (CCS-MPC). In FS- MPC, a finite number of control actions (switching states of inverter) are used, whereas in CCS-MPC, the number of control actions depends on the prediction horizon.

In this paper, the 3L-NPC will be controlled using FS-MPC scheme has been adopted with considering three main control objectives. These control objectives are- current tracking error, neutral point voltage balancing and number of switching states transition for reduction of average switching frequency. As, the switching frequency term has been added in the cost function, the algorithm will be convoluted in nature for selecting proper weighting factor of different control objectives. The main objectives of this research work are-

- To select proper weighting factor for the control objectives.
- To analyze switching loss.
- To analyze the effect of adding switching frequency term on the current THD and neutral point voltage balancing.

This research work has been presented in this paper into four sections. The 3L-NPC operation along with mathematical model as well as the FCS-MPC control scheme design for the reduction of switching frequency are explain in section 2. In section 3, Simulation results and performance evaluation of the proposed system are given. The concluding remarks are given in section 4.

## 2. RESEACH METHODOLOGY

This section is designed in the following sub-section. These are system modelling, discrete-time model, controller design.

#### 2.1. System modelling

Three phase three level NPC voltage source inverter consists of three legs and each leg consisting four semiconductor switches with antiparallel diode as shown in figure 1. The lower two switches are complementary to the upper two switches. The switching states of 3L- NPC has been given in the table 1.



Fig 1: Circuit diagram of 3L-NPC

 Table 1. Switching state for 3L-NPC inverter

$\mathbf{S}_{\mathbf{x}}$	$S_{x2}$	$\mathbf{S}_{\mathbf{x}2}$	S <sub>x3</sub>	$S_{x4}$	$V_{x0}$
+	1	1	0	0	$V_{dc}/2$
0	0	1	1	0	0
-	0	0	1	1	-V <sub>dc</sub> /2

In table 1 x = {a, b, c} corresponds to the three phases so there will be  $3^3 = 27$  voltage vectors available. Here,  $V_{dc}$  represents the DC voltage source. Based on their amplitudes, the voltage vectors are classified into three groups, such as small  $(V_{7,...}V_{18})$ , zero  $(V_0)$ , and medium  $(V_{1...}V_6)$  vectors. The redundant vector states are accumulated into a single block as shown in figure 2. Redundant vectors basically help in balancing the capacitor voltage.



Fig 2: Voltage vectors generated by 3 level NPC inverter

### 2.2 Modelling of Load

The load modelling is necessary after designing the converter model. The three-phase voltage  $(v_{aN}, v_{bN}, v_{cN})$  of both simplified and conventional NPC can be expressed as

$$v_{aN} = L\frac{di_a}{dt} + Ri_a + v_{nN} \tag{1}$$

$$v_{bN} = L\frac{d\iota_b}{dt} + Ri_b + v_{nN} \tag{2}$$

$$v_{cN} = L\frac{ai_c}{dt} + Ri_c + v_{nN} \tag{3}$$

where, the resistance and inductance of the load are indicated by R and L. The output voltage vector can be presented as

$$\mathbf{v} = \frac{2}{3} \left( V_{aN} + a \times V_{bN} + a^2 \times V_{cN} \right)$$
(4)

Therefore, the dynamic load current equation can be expressed as

$$\mathbf{v} = R\mathbf{i} + L\frac{d\mathbf{i}}{dt} \tag{5}$$

For predicting the future load current and capacitor voltage at k-th time from measured voltage and current, discrete time model is essential. For the estimation of predictions, numerous discretization models are available. The discrete time model is designed here by utilizing forward Euler approximation and the derivative of load current is expressed as

$$\frac{di}{dt} \approx \frac{i(k+1)-i(k)}{T_s}$$
(6)

The predictive load current at (k + 1) time can be determined by replacing the Eqn. (9) to Eqn. (8) and can be expressed as

$$i^{p}(k+1) = \left(1 - \frac{RT_{s}}{L}\right)i(k) + \frac{T_{s}}{L}V(k)$$
(7)

The superscript *P* denotes the predicted variables. Where,  $i^{p}(k+1)$  denotes predicted load current.

#### **2.3 Cost Function Design**

To reduce the error between the reference and measure current and the difference of two dc link capacitor voltage, a cost function is designed and it is expressed as

$$g = \left| i_{\alpha}^{*}(k+1) - i_{\alpha}^{p}(k+1) \right| + \left| i_{\beta}^{*}(k+1) - i_{\beta}^{p}(k+1) \right| + \lambda_{dc} |V_{c1}(k+1) - V_{c2}(k+1)| + \lambda_{sw} n_{st}$$
(8)

The real component of reference and predictive current are presented by  $i^*_{\alpha}(k+1)$ , and  $i^p_{\alpha}(k+1)$ , respectively and  $i^p_{\beta}(k+1)$  and  $i^*_{\beta}(k+1)$  indicates the imaginary component of predictive and reference load current. The predictive dc link capacitor voltages at time (k+1) are presented by  $V_{c1}(k+1)$  and  $V_{c2}(k+1)$ . These two terms are summed together by utilizing a weighting factor  $\lambda_{dc}$ . The effect of switching frequency current THD is also investigated in this paper. To reduce switching frequency number of switching transition,  $n_{st}$  is added in the cost function along with weighting factor,  $\lambda_{sw}$ .

## 3. CONTROL STRATEGY

The flow chart of the MPC based control strategy for 3-L NPC is shown in Figure 3. It has been seen that the flow chart contains two loops, one is inner and the other is the outer loop. The inner loop is executed for all possible voltage vectors and the outer loop is executed to determine the

optimum switching state for the next sampling period.

The overall control strategy can be summarized by the following sequences:

**Step 1:** The Load current (k) and capacitor voltages  $V_{c1}(k)$  and  $V_{c2}(k)$  are measured.

**Step 2:** The future load current  $i^p(k+1)$ , capacitor voltages  $V_{cl}(k+1)$ ,  $V_{c2}(k+1)$  and  $n_{st}$  are predicted for all the possible switching states and selection optimal g.

Step 3: The optimal voltage vector v (k) is applied.

#### 4. RESULTS AND DISCUSSION

The simulation of the conventional 3L-NPC VSI for passive loads has been performed using MATLAB-Simulink. The configuration parameters of the system are shown in Table 3.

Table 3 Si	imulation	Parameters
------------	-----------	------------

Parameters	Values [unit]
Load resistance, R	10 [Ω])
Load inductance, L	10 [mH]
DC link capacitor, C	3300 [µF]
DC link voltage, $V_{dc}$	520 [V]
Reference current, I <sub>ref</sub>	10 [A]
Reference frequency, f <sub>ref</sub>	50 [Hz]
Sampling Time, T <sub>s</sub>	25 [µs]

The optimum point selection method has been shown in the Fig. 4 below. The optimum point is basically chosen by taking other weighting factor as constant and by tuning the weighting factor of the switching frequency term.

From Fig. 4, it is evident that the switching frequency is reduced by a margin of 73.9% at the optimum point of  $\lambda_{sw}$ = 0.158 sacrificing current THD of 0.10%. The switching frequency at this point is around 2.46 KHz which is in acceptable limit. Moreover, without the optimum point selection it is near about 9.43 KHz which is quite high. So, this method effectively reduce the switching frequency which also reduces the switching loss. The switching loss is shown in Table 4.

Table 4: Switching loss reduction and current THD

Operation Condition	Switching loss [W]	Current THD [%]
Normal	1.88	1.35
Optimum	0.56	1.45

It is obvious that around 70% of switching loss is reduced using the proposed method. Moreover, the current THD is still maintained the IEEE standard.

The three phase output current response and neutral point voltage balancing waveforms are represented by Fig. 5 and Fig. 6 respectively.



Fig. 5: Three phase output current waveforms.

By observing Fig. 5, it is obvious that the current tracks the reference current smoothly. The quality of the output current is verified by the FFT analysis which gives us around 1.45% THD.



Fig. 6: Neutral point voltage waveforms.



Fig. 4: Optimum point selection methodology.

# 5. CONCLUSION

In this paper, novel approach to reduce switching frequency without affecting that much on the current THD and neutral point voltage balancing portion of a NPC inverter system. In our proposed control scheme, 73.9% reduction of switching frequency has been achieved while sacrificing current THD of 0.10% which is in the acceptable range. The neutral point voltage is also perfectly balancing by the proposed system. Other power loss analysis namely conduction, harmonic loss is required to clarify the controller performance.

### 6. ACKNOWLEDGMENTS

We would like to thank all faculties of the dept. of EEE, JUST for their kind co-operation to fulfil this paper successfully.

#### 7. REFERENCES

- B. Wu and M. Narimani, "High-power converters and AC drives". IEEE-Wiley Press, 2017.
- [2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B.Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [3] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S.Kouro, "Multilevel voltage source- converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007

- [4] M. Saeedifard, P. M. Barbosa, and P. K. Steimer, "Operation and control of a hybrid seven-level converter," IEEE Trans. on Power Electron., vol. 27, no. 2, pp. 652–660, 2012.
- [5] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, "Multilevel voltage source- converter topologies for Inverter Type Simplified 3L-NPC Conventional 3L-NPC industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
- [6] Ahoora Bahrami, Mehdi Narimani. "A New Five Level T-type Nested Neutral Point Clamped (T-NNPC) Converter", IEEE Trans. on Power Electron., 2019.
- [7] Bahrami A, Narimani M (2019) A New Five Level Ttype Nested Neutral Point Clamped (T-NNPC) Converter. IEEE Trans. on Power Electron.
- [8] S. Kouro, J. Rebolledo, J. Rodriguez, "Reduced Switching-Frequency-Modulation Algorithm for High-Power Multilevel Inverters", *IEEE Transactions on Industrial Electronics*, 54, No. 5, 2894-2901, 2007.
- [9] M. perindl, E. Schaltz, P. Thogersen, "Switching Frequency Reduction Using Model Predictive Direct Current Control for High-Power Voltage Source Inverters", *IEEE Transactions on Industrial Electronics*,58 No. 7, 2826-2835, 2011.