Gain and Bandwidth Enhancement in CMOS Low-Voltage Low-Power Operational Amplifiers

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ABSTRACT
In this paper, a low-voltage low-power CMOS operational amplifier using the composite cascode technique is presented. This technique has been employed in the differential input pair and output transistors to enhance the gain of op-amp. Also, indirect compensation is used to improve the frequency response of the op-amp and avoids instability when a large capacitive load at the output of the op-amp must be handled. Two-stage op-amp is designed and simulated in a TSMC 0.18 µm CMOS technology, to evaluate the proposed technique. The sub-threshold region is employed in the design to use the low supply voltage and reduce power consumption effectively. The op-amp operates at a 0.7 V power supply with 891 nW power consumption. The open-loop gain is 90.1 dB, the unity gain-bandwidth (UGBW) is 309 kHz, and the phase margin is 57.6 degree under 15 pF load.

Keywords
Low-Voltage, Low-Power, Op-amp, Composite cascode, Indirect compensation, DC gain, Unity gain-bandwidth.

1. INTRODUCTION
During the last few years, the demand for low-voltage and low-power portable electronic equipment has increased significantly, and the operational amplifier is one of the most important analog blocks in this equipment. So, the continuous work and research in the field of low-voltage low-power op-amps are very significant to keep up with the developments in IC design. The need for high gain and high bandwidth op-amps exists for many systems such as pipeline A/D converters and sigma-delta converters. However, in the low-voltage and low-power design, the gain and bandwidth of the op-amp are limited by minimum voltages and currents. Gain and bandwidth enhancement techniques are necessary for designing a high gain and high bandwidth op-amp.

Various gain boosting techniques have been used to design high gain op-amps [1]–[6]. In [1] show how positive feedback can be used to enhance the DC gain of an op-amp without sacrificing the settling time or the frequency response. In [2] fully differential gain-boosted folded-cascode op-amp is designed. The basic op-amp is a fully differential folded-cascode op-amp with switched-capacitor common-mode feedback (SC-CMFB). Two fully differential folded-cascode op-amps with continuous-time CMFBs are utilized as auxiliary op-amps to enhancement the DC gain of the basic op-amp. In [3], a new gain enhancement technique called "body-driven gain boosting" is proposed. "Body-driven gain boosting" amplifiers have been used for common gate-driven op-amps to increase the DC gain. Composite cascode connection for the input differential stage of op-amps has been used [4]–[6] to achieve high voltage gain. The advantages of the composite cascode op-amp include easiness of layout, small cell size (needing minimum compensation capacitor), and low-supply current drain. Different frequency compensation techniques for two-stage operational amplifiers have been reported [7]–[13]. In [7], the authors presented a novel technique for indirect Miller compensation, which uses the bulk as an input to reduce the device count for creating necessary feedback signals in the indirect compensation method. In [8-11], a new frequency compensation technique called indirect frequency compensation for two/multi-stage op-amps is proposed. The indirect compensation results in much faster and low-power op-amps, a significant reduction in the layout size, and better power supply noise rejection (PSRR). In [12], an improved frequency compensation technique known as Ahuja compensation (cascade compensation) is presented. This technique provides stable operation for a much more extensive range of capacitive loads. In [13], the authors proposed a new compensation technique based on the current buffer. This technique provides high unity-gain bandwidth and better PSRR performance.

In this paper, the proposed op-amp topology applies the composite cascode technique in both the input and the output stages to increase the DC gain. Also, indirect compensation is used to achieve high unity gain-bandwidth and stable operation for a much larger range of capacitive loads. The organization of this paper is as follows. In section 2, the sub-threshold operation is presented. In sections 3 and 4, the composite cascode technique and indirect compensation are discussed, respectively. The structure of the proposed op-amp is described in section 5. The simulations results are provided in Section 6, and finally, the conclusion is given.

2. SUB-THRESHOLD OPERATION
The operation of the MOS device in the sub-threshold region is very important when low power circuits are desired. When the V_{GS} in the MOS transistor is less than the threshold voltage (V_{th}), the MOSFET works in the sub-threshold region. The drain current I_D of a MOS transistor in the sub-threshold region is based on the channel diffusion current and can be given by (1) when referred to source voltage [14].

$$I_D = I_S \left(\frac{W}{L}\right) exp\left(q\frac{V_{GS}-V_{th}}{nKT}\right)\left[1-exp\left(-q\frac{V_{DS}}{KT}\right)\right] \quad (1)$$

Where I_S is the characteristic current, T is the absolute temperature, n is the slope factor, K is the Boltzmann constant, and q is the charge of the electron or hole. If $V_{DS} \geq 3KT/q$, then the transistor will be saturated in the sub-threshold region. The transconductance g_m can be found as presented in (2), which is a function of current I_D and factor nKT/q [14].

$$g_m = q\frac{I_D}{nKT} \quad (2)$$

There is a linear relationship between transconductance and current. Also, transconductance is independent of device geometry. However, in a strong inversion relationship

between transconductance and current is square law and also a function of device geometry. The body-effect transconductance g_{mb} can define as [14]:

$$g_{mb} = g_m \frac{\lambda}{2\sqrt{2\emptyset_f + V_{SB}}} \quad (3)$$

3. COMPOSITE CASCODE

The composite cascode technique is used in the design of operational amplifiers to achieve high gain at low-power. The structure of a conventional cascode amplifier and a composite cascade amplifier are shown in Fig. 1. In the composite cascade amplifier, both gates of transistors M1 and M2 are connected to the input signal and have an equal dc bias source (V_{GG}) [15]. In the composite cascode amplifier, if M2 is selected with a higher aspect ratio than M1, with a proper bias of V_{GG} and I_{bias}, M1 is set in the strong inversion region while M2 is operating in the sub-threshold region. As a result, the gain can be increased. However, the bandwidth is lower than the conventional cascode amplifier [15].

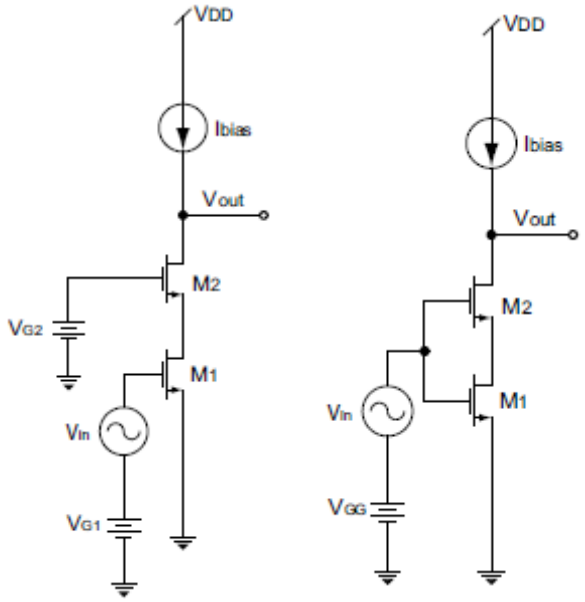


Fig 1: (a) Conventional cascode amplifier, (b) Composite cascode amplifier [15].

Assuming the current source has infinite output impedance, the output resistance of both amplifiers is [15]:

$$r_{out} = r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2} \quad (4)$$

Where r_{oi} is the output resistance of transistor M_i, g_{mi} denote the transconductance of the transistor M_i and g_{mbi} represents body-effect transconductance of the transistor M_i. The voltage gain of the circuit of Fig. 1 (a) is:

$$|A_O| = [g_{m1} r_{o1} + g_{m1} r_{o1} (g_{m2} + g_{mb2}) r_{o2}] \quad (5)$$

Also, the voltage gain of the circuit of Fig. 1 (b) is:

$$|A_O| = [g_{m1} r_{o1} + g_{m2} r_{o2} + g_{m1} r_{o1} (g_{m2} + g_{mb2}) r_{o2}] \quad (6)$$

According to Equations (5) and (6), composite cascode amplifier has higher gain compared with the conventional cascode amplifier.

For the composite cascode amplifier, if the current source load has a finite resistance (R), the voltage gain is [15]:

$$|A_O| = \frac{[g_{m1} r_{o1} + g_{m2} r_{o2} + g_{m1} r_{o1} (g_{m2} + g_{mb2}) r_{o2}]}{1 + \frac{1}{R}[r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o1} r_{o2}]} \quad (7)$$

4. INDIRECT COMPENSATION

In indirect compensation or indirect feedback frequency compensation, the compensation capacitor is connected to an inner low impedance node (v_x) in the first stage, which allows indirect feedback of the compensation current from the output node to the inner high-impedance node (the output of the first stage, i.e., node (1)) [8], [11].

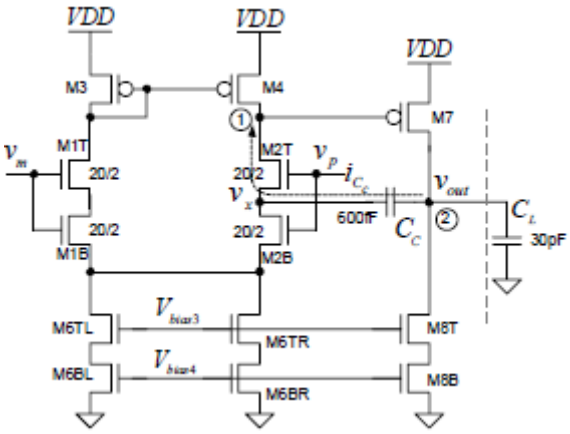


Fig 2: Two-stage op-amp topology with indirect compensation [8].

The current feedback (i_{C_c}) through the compensation capacitor (C_c) can be approximated as [8]:

$$i_{C_c} \approx v_{out}/(1/j\omega C_c) \quad (8)$$

An op-amp with indirect compensation technique, the dominant pole location is the same as in Miller compensation. While, instead of an RHP zero, the op-amp have an LHP zero located at [8]:

$$f_z = \frac{g_{mc}}{2\pi(C_c + C_{v_x})} \quad (9)$$

Where g_{mc} is the transconductance of the common-gate amplifier and C_{v_x} is the capacitance connected to the low impedance node (v_x).

5. THE STRUCTURE OP PROPOSED OP-AMP

The structure of the low-voltage low-power operational amplifier using the composite cascode technique is shown in Fig. 3. This technique has been applied to the differential input pair (M1, M2, M3, and M4) and output transistors (M11, M12, M13, and M14) to achieve high gain. Also, the transistors M91, M101, M92, and M102 are implemented with a composite cascode technique. Two indirect compensation techniques are used to increase the unity-gain bandwidth. The size of transistors, Capacitors, and reference current are shown in Table 1.

Table 1. The Size of transistors, Capacitors, and Reference Current

	Composite cascode input
M1-M2	(W/L) 22um/1um
M3-M4	(W/L) 80um/1um
M5-M6	(W/L) 1um/1um
M7-M8	(W/L) 26um/1um
M101-M91	(W/L) 1.1um/1.97um
M102-M92	(W/L) 60um/2um
M11	(W/L) 20um/1um
M12	(W/L) 44um/1um
M13	(W/L) 52um/1um
M14	(W/L) 13.8um/1um
M15	(W/L) 1.2um/1um
M16	(W/L) 1um/1um
Indirect Compensation	Cc1=0.2pF, Cc2=0.6 pF
Load Capacitance (CL)=15 pF & **Iref**=70 nA	

The following equations calculate the small-signal DC gain of the proposed op-amp.

The DC gain of the first stage is:

$$|A_1| = (g_{m8} + g_{mb8}).(R_{o10} \parallel R_{o8}) \quad (10)$$

Where,

$$R_{o10} = r_{o101} + r_{o102} + g_{m102} r_{o101} r_{o102} \quad (11)$$

$$R_{o8} = r_{o8}[1 + (g_{m8} + g_{mb8}).([r_{o1} + r_{o3} + g_{m3} r_{o1} r_{o3}] \parallel r_{o6})] \quad (12)$$

The DC gain of the second stage is:

$$|A_2| = G_{m14}\,(R_{o12} \parallel R_{o13}) \quad (13)$$

$$G_{m14} = = \frac{[g_{m14} r_{o14} + g_{m13} r_{o13} + g_{m14}(g_{m13} + g_{mb13}) r_{o13}}{R_{out}} \quad (14)$$

Also, R_{o12} and R_{o13}can be calculated similarly to equation (10). Finally, the total DC gain is:

$$|A_0| = A_1 . A_2 \quad (15)$$

The proposed circuit has three poles, which can be obtained as follows. The first pole,

$$P_1 = -\frac{1}{C_1 R_1}$$

$$C_1 = C_{gd92} + C_{gb8} + C_{gb7} + C_{db7} + C_{gs7} + C_{gs8} + C_{gd8}(1 - A_1) \quad (16)$$

$$R_1 = \frac{1}{g_{m7}}$$

The second pole,

$$P_2 = -\frac{1}{C_2 R_2}$$

$$C_2 = C_{gd8} + C_{db8} + C_{gd102} + C_{gb13} + C_{gb14} + C_{gs14} + C_{gd13}(1 - A_2) + C_{gd14} + C_{gs13} \quad (17)$$

$$R_2 = R_{o10} \parallel R_{o8}$$

And the third pole,

$$P_3 = -\frac{1}{C_3 R_3}$$

$$C_3 \approx C_L + C_{C1} + C_{C2} \quad (18)$$

$$R$$

6. SIMULATION RESULTS

The proposed op-amp is simulated in the HSPICE software with a 0.7 volt power supply in the TSMC 0.18µm 1P6M CMOS technology. The result of the DC analysis shows that the power consumption of the proposed scheme is 891 nW.

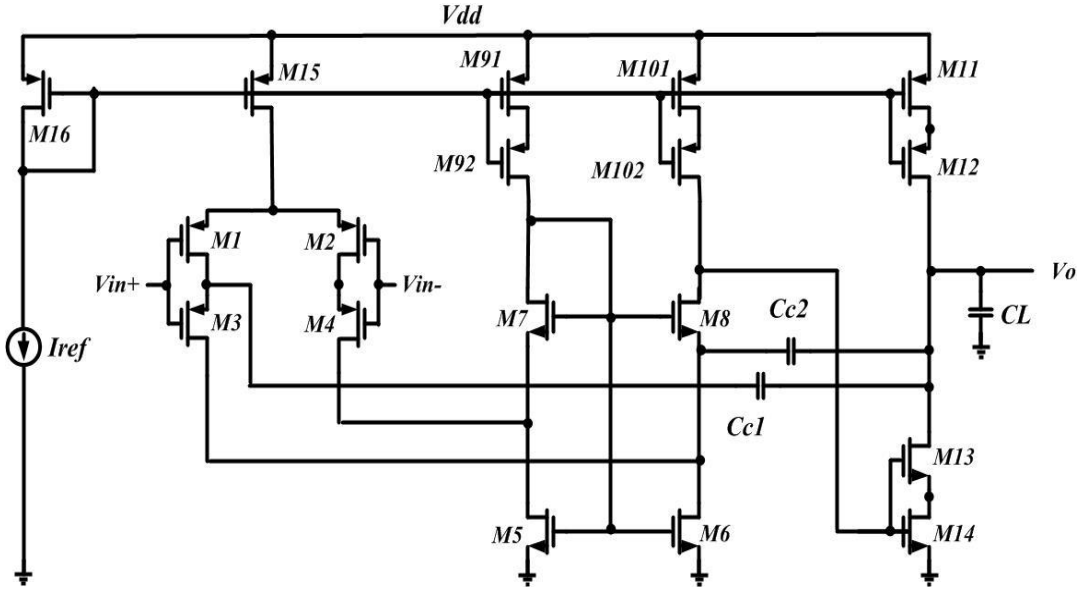


Fig 3: The proposed op-amp using composite cascode technique and indirect compensation.

6.1 DC gain, phase margin, unity-gain bandwidth

The simulated open-loop gain, phase margin, and unity gain-bandwidth are shown in Fig. 4. The simulation result shows the open-loop gain is 90.1 dB, the unity gain-bandwidth is 309 kHz, and the phase margin is 57.6 degree.

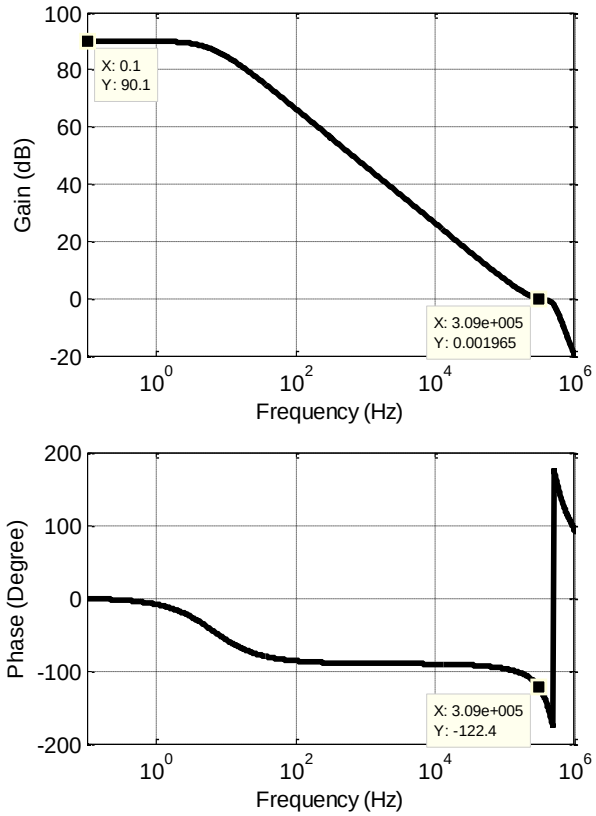


Fig 4: The open-loop frequency response of the op-amp under 15 pF load.

6.2 CMRR

The efficiency and quality of an amplifier are determined by the Common Mode rejection Ratio (CMRR). The high CMRR is very useful in types of equipment like instrumentation devices. The CMRR in dB is derived from the following equation. Fig. 5 shows the simulation result of the CMRR. The CMRR of the op-amp is 100.3 dB @ 10 Hz.

$$CMRR(dB) = Av_{DM}(dB) - Av_{CM}(dB) \quad (19)$$

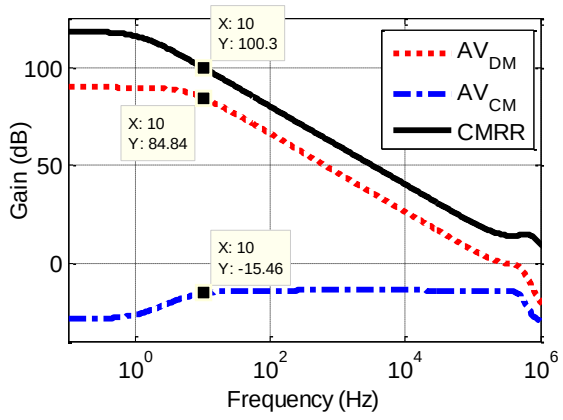


Fig 5: The CMRR result.

6.3 Slew Rate

The slew rate of an op-amp is the rate of change in output voltage affected by a step-change in the input. The simulation result of the slew rate is shown in Fig. 6. The slew rate of the proposed op-amp is 65.52 V/ms.

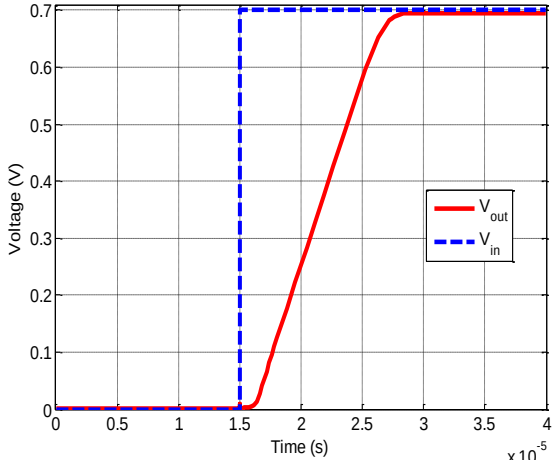


Fig 6: The slew rate result.

6.4 Noise

In the MOSFET devices, there are two crucial noise sources, which are the flicker noise (below 1 MHz) and the thermal noise. Fig. 7 shows the device noise as a function of frequency. First, the noise follows a $1/f^{v}$ dependence and is referred to as flicker noise ($v \cong 0.8 - 1.2$) or $1/f$ noise. Above the corner frequency (f_c) the noise is typically frequency independent (thermal and shot noise). Above the second characteristic frequency (f_c') the noise increases sharply due to parasitic capacitances coupling noise between different regions of the device [16].

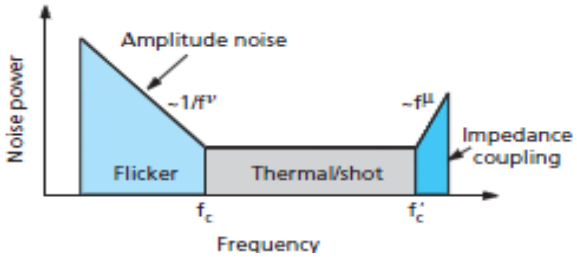


Fig 7: Power spectral density of flicker noise and thermal noise [17].

The simulated input-referred voltage noise performance of the op-amp is shown in Fig. 8. The input-referred noise is 1.569 nV/√Hz at 1 Hz and 18.9 pV/√Hz at 100 Hz.

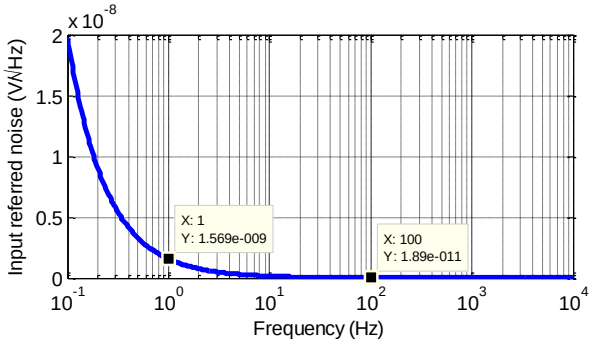


Fig 8: Input-referred noise.

6.5 Other simulation results

The effect of supply voltage variation on open-loop gain and phase margin is shown in Fig. 9. According to this figure, the designed circuit has the same performance as the supply voltage variation.

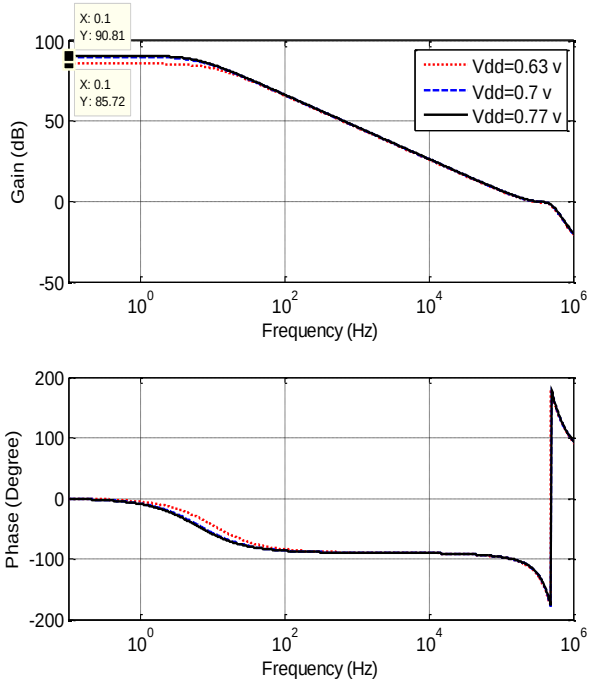
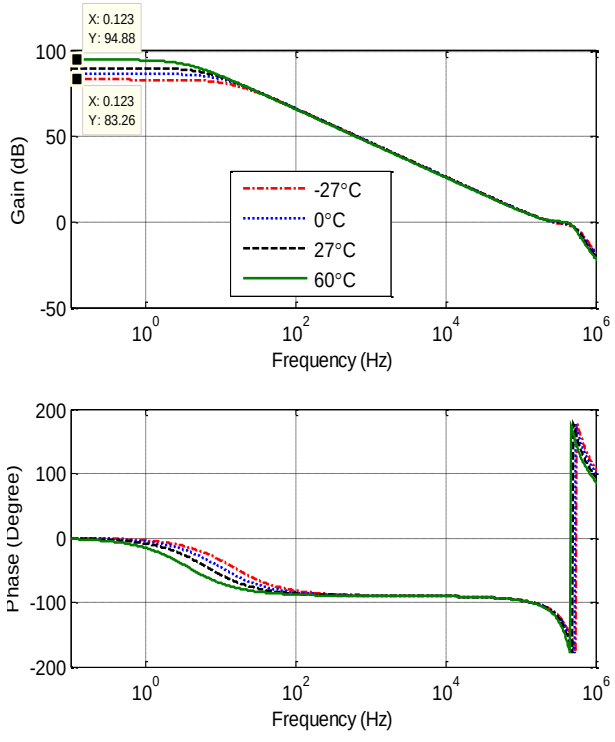
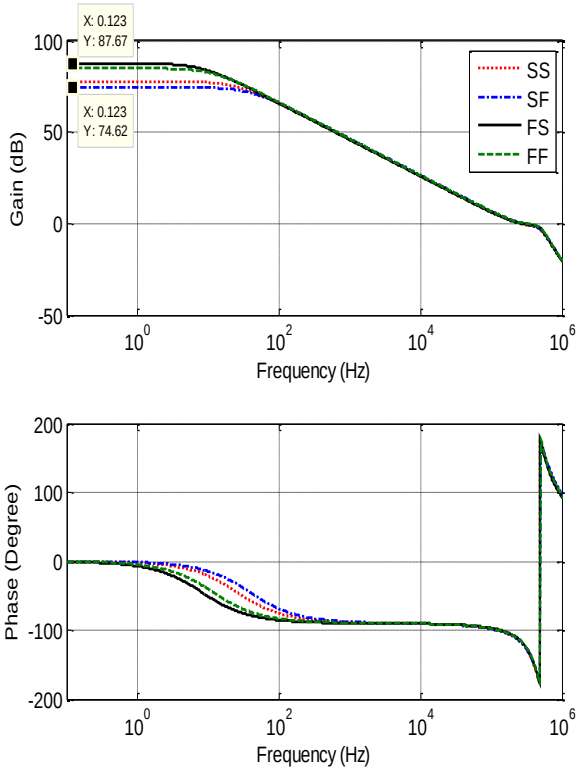


Fig 9: Effect of supply voltage variation on open-loop gain and phase margin.

In Fig. 10, the open-loop gain and phase margin are shown in different temperatures and process corners. As can be seen, the designed circuit at the different temperatures and process corners works well.



(a)



(b)

Fig 10: The open-loop gain and phase margin. (a) Effect of different temperatures, (b) Effect of process corners.

6.6 Comparison of the proposed amplifier

In Table 2, the proposed op-amp is compared with other operational amplifiers. Two figure of merit (FOM) can be defined as [18], [19] to evaluate this work:

$$FOM_1 = \frac{Gain\ (dB) * UGBW\ (kHz)}{Power\ supply\ (mV) * Power\ consumption\ (\mu W)} \quad (20)$$

$$FOM_2 = \frac{Slew\ Rate\ (\frac{V}{\mu s}) * C_L(pF)}{Power\ consumption\ (\mu W)} \quad (21)$$

7. CONCLUSION

In this paper, a low-voltage low-power two-stage op-amp with composite cascode technique to achieve high DC gain is designed and simulated. The proposed op-amps utilize indirect compensation to increase the unity gain-bandwidth. Also, to reduce power consumption and use low supply voltage, the sub-threshold region is employed. Simulation results have been presented to confirm the considerable improvement in DC gain and unity-gain bandwidth. The op-amp operates at a 0.7 V power supply with 891 nW power consumption. The simulation result shows the open-loop gain is 90.1 dB, the unity gain-bandwidth is 309 kHz, and the phase margin is 57.6 degree. The proposed op-amp shows a considerable FOM than other op-amps.

8. REFERENCES

[1] M. E. Schlarmann, S. Q. Malik, and R. L. Geiger, "Positive Feedback Gain-Enhancement Techniques for Amplifiers Design," IEEE International Symposiums on Circuits and Systems, Vol. 2, pp. 37-40, 2002.

[2] SU Li, and Qiu Yulin, "Design of a Fully Differential Gain-boosted Folded-Cascode Op Amp with Settling Performance Optimization," IEEE Conference on Electron Devices and Solid-State Circuits, pp. 441-444, 2005.

[3] S. A. Zabihian, and R. Lotfi, "A Sub-1-V High Gain Single Stage Operational Amplifier," IEICE Electronics Express, Vol. 5, No.7, pp. 211-216, 2008.

[4] D. J. Comer, D. T. Comer, and R. P. Singh, "A High-gain, Low-power CMOS Op Amp using Composite Cascode Stages," in Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems, 600–603, 2010.

[5] R. P. Singh, D. J. Comer, T. Waddel, D. T. Comer, and K. Layton, "High-gain microwatt composite cascode op amps," International Journal of Electronics, Vol. 99, No. 9, pp. 1179-1190, 2012.

[6] D. T. Comer, D. J. Comer, and L. Li, "A high-gain complementary metal-oxide semiconductor op amp using composite cascode stages," International Journal of Electronics, Vol. 97, No. 6, pp. 637-646, 2010.

[7] A. Esmaili, H. Babazadeh, Kh. Hadidi, and A. Khoei, "Bulk Driven Indirect Feedback Compensation Technique for Low-Voltage Applications," 21st Iranian Conference on Electrical Engineering, pp. 1-5, 2013.

[8] V. Saxena, and R. Baker, "Indirect feedback compensation of CMOS op-amps," IEEE Workshop on Microelectronics and Electron Devices, pp. 3-4, 2006.

[9] V. Saxena and R. Baker, "Indirect compensation techniques for three-stage CMOS op-amps," 52nd IEEE International Midwest Symposium on Circuits and Systems, pp. 9-12, 2009.

[10] V. Saxen,a and R. Baker, "Indirect compensation techniques for three-stage fully-differential op-amps," 53rd IEEE International Midwest Symposium on Circuits and Systems, pp. 588-591, 2010.

[11] V. Saxena, and R. Baker, "Indirect Compensation Technique for Low-Voltage Op-Amps," in Proceedings of the 3rd Annual Austin Conference on Integrated Systems and Circuits, pp. 1-4, 2008.

[12] K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers", IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 6, pp.629-633, 1983.

[13] G. Palmisano, and G. Palumbo, "A Compensation Strategy for Two-Stage CMOS OPAMS Based on Current Buffer," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Vol. 44, No. 3, pp. 252–262, 1997.

[14] Gh. Moradi, M. R. Alamdar, and S. Izadpanah Toos, "Hybrid Frequency Compensation to Improve Unity-Gain Bandwidth of Low-Voltage Low-Power CMOS Operational Amplifiers," Majlesi Journal of Telecommunication Devices, Vol. 7, No. 2, pp. 65–72, 2018.

[15] L. Li, "High Gain Low Power Operational Amplifier Design and Compensation Techniques," Ph.D. Thesis, Brigham Young University, 2007.

[16] A. Soltani, M. Yaghmaie, B. Razeghi,R. Pourandoost, S. Izadpanah Tous, and Abbas Golmakani, "Three stage low noise operational amplifier design for a 0.18 um CMOS process," 9th International Conference on Electrical Engineering, Computing Science and automatic Control (CCE), 2012 .

[17] Samuel Martin, Vance D. Archer III, David M. Boulin, Michel R. Frei, Kwok K. Ng, and Ran-Hong Yan , "Device Noise in Silicon RF Technologies," Bell Labs Technical Journal, Summer 1997.

[18] E. Kargaran, M. Sawan, Kh. Mafinezhad, H. Nabovati, "Design of 0.4V, 386nW OTA Using DTMOS Technique for Biomedical Applications," 55th IEEE International Midwest Symposium on Circuits and Systems, pp. 270–273, 2012.

[19] M. R. Valero, S. Celma, N. Medrano, B. Calvo, and C. Azcona, "An Ultra Low-Power Low-Voltage Class AB CMOS Fully Differential OpAmp," IEEE International Symposium on Circuits and Systems, pp. 1967-1970, 2012.

[20] A. Tanaka, Z. Qin, H. Yoshizawa, "A 0.5-V 85-nW rail-to-rail operational amplifier with a cross-coupled output stage," IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS), pp. 137-140, 2013.

[21] M. R. Valero Bernal, S. Celma, N. Medrano and B. Calvo, "An ultralow-power low-voltage class-AB fully differential OpAmp for long-life autonomous portable equipment," IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 59 , No. 10 , pp. 643-647, 2012.

[22] M. Razzaghpour, and A. Golmakani, "An ultra-low-voltage ultra-low power OTA with improved gain-bandwidth product," International Conference on microelectronics, pp. 39-42, 2008.

[23] S. A. Zabihian, and R. Lotfi, "Ultra-low-voltage, low-power, high-speed operational amplifiers using body-driven gain-boosting technique," IEEE International Symposium on Circuits and System, pp. 705- 708, 2007.

Table 2. The Size of transistors, Capacitors, and Reference Current

	proposed	**[20]**	**[21]**	**[22]**	**[23]**
Technology (µm)	0.18	0.18	0.18	0.18	0.18
Power supply (mV)	700	500	800	500	700
Power consumption (µW)	0.891	0.085	1.2	1.02	82
Gain (dB)	90.1	101	51	88.5	74.2
Phase margin (Degree)	57.6	50.59	60	66.3	76.5
Unity gain-bandwidth (kHz)	309	8.6	57	83.88	25000
CMRR (dB)	100.3@ 10 Hz	90 @ DC	-----	133.85	-----
PSRR (dB)	120.6 @ 10 Hz	-----	-----	-----	-----
Slew Rate (V/µs)	0.065	-----	0.14	0.052	13
Input referred noise ($nV/\sqrt{Hz}$)	1.569 @ 1 Hz	-----	-----	-----	-----
C_{Load} (pF)	15		8	15	3
FOM_1 & FOM_2	44.63 & 1.09	20.44 & 0.18	3.03 & 0.93	14.47 & 0.76	32.32 & 0.47