Abstract

Static Random Access Memory (SRAM) is a volatile memory that is widely used in every embedded system – Silicon on Chip (SoC), Digital Signal Processing (DSP), Microcontroller, Field Programmable Gate Array (FPGA) and Video applications. It is also used in register, cache and cache-less applications due to large storage density, reduced read-write access time, low power consumption and stability. Thus, this paper presents the design principle of SRAM at the 45nm technology node, the peripheral building blocks and functionalities, operations, transistor scalene challenges, and process variation effects of SRAM designs. A clear detail schematic diagrams using Cadence Virtuoso design tool for IC design was used for designing the peripheral circuitry and the SRAM cell.

References

1. Ezeogu, Apollos. 2013 “Process Variation Aware Non-Volatile (Memristive) 9T SRAM Memory Design in Nano-CMOS Technologies”, M.Sc. Theses submitted to University of Bristol,
United Kingdom.

2. Uddalak Bhattachara et al., 2008 “45nm SRAM Technology Development and Technology Lead Vehicle” Intel Technology Journal, Volume 12, Issue 2


7. Hoang Anh Du Nguyen, Lei Xie, Mottaqiallah Taouil, Razvan Nane, Said Hamdioui, Koen Bertels, 2015 “Computation-In-Memory Based Parallel Adder” Laboratory of Computer Engineering, Faculty of EE, Mathematics and CS Delft University of Technology, Mekelweg 4, 2628 CD Delft, The Netherlands.


**Index Terms**

Computer Science

Circuits and Systems

**Keywords**

Memory cell, Embedded System, Read, Write, Process variation, Leakage current, Power consumption.