High Efficiency Class F Power Amplifier Design for GSM System

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ABSTRACT
Due to the high increase in and demand for a wide assortment of applications that require low-cost, high-efficiency, and compact systems, RF power amplifiers are considered the most critical design blocks and power consuming components in wireless communication, TV transmission, radar, and RF heating. Therefore, much research has been carried out in order to improve the performance of power amplifiers. This paper presents the design and analysis of Class F power amplifier. The Class F amplifier is used in a base station for mobile system because of its high efficiency. An implementation of high efficiency class-F power amplifier with Gallium Arsenide (GaAs) Field Effect Transistor (FET) was realized in this paper. The analysis and design of Class F power amplifier were studied at different operating frequency. It is found that the amplifier can operate at GSM and CDMA base station at input power level more than 15dBm. The simulation of the class-F power amplifier circuit model was undertaken using Agilent's Advanced Design system (ADS).

General Terms
Wireless communication, Base Station, Advanced Design System, and GSM and CDMA communication systems.

Keywords
Power Amplifier (PAs), Class F power amplifier , Gallium Arsenide (GaAs FET).

1. INTRODUCTION
The Mobile communication has become quite common in today's world with the increasing needs of effectively utilized bandwidth, and efficient and compact device technologies. The information can be easily communicated by mobile communication system such as GSM and CDMA. The modern wireless communication industry has increased interest for the high-efficient and linear amplifiers to accommodate current communication standards [1].

RF Power Amplifiers (PAs) are used in a wide variety of applications including wireless communication, TV transmissions, radar and RF heating. The basic techniques for RF PAs can use classes as A, B, C, D, E, and F for frequencies ranging from very low frequency through microwave frequencies. It is a critical element in transmitter units of communication systems, is expected to provide a suitable output power can range from depend by application. The output power from a PA must be sufficient for reliable transmission with a good gain, high efficiency and linearity. High gain reduces the number of amplifier stages required to deliver the desired output power and hence reduces the size and manufacturing cost. High efficiency improves thermal management, battery lifetime and operational costs. Good linearity is necessary for bandwidth efficient modulation [2].

Power amplifiers efficiency is enhanced by operating the transistor in different classes. Class-F PAs offer high power capabilities and high efficiency with a limited number of controlled harmonics [2]. In an ideal class-F PA the efficiency is 100% and is achieved by using an infinite number of harmonics to yield square and half-wave sinusoid waveform shapes at device drain for the voltage and current respectively.

Typically, only one or two harmonics are controlled at a time, the second and/or third-harmonic, with a maximum theoretical efficiency of 81.65% when using an ideal device and the required impedances at each harmonic and fundamental-frequency (f_0), the ideal class F power amplifier presented as shown in Fig 1.

Class-F output network designs have been reported in the literature using transmission lines as harmonic resonators where electrical lengths are practical [2]. Also, the classic class-F PA design has addressed output networks built based upon lumped-element resonators to peak one harmonic frequency and a shunt connected tank circuit tuned at f0 [3]. However, when a real device is used, parasitic act against this design methodology.

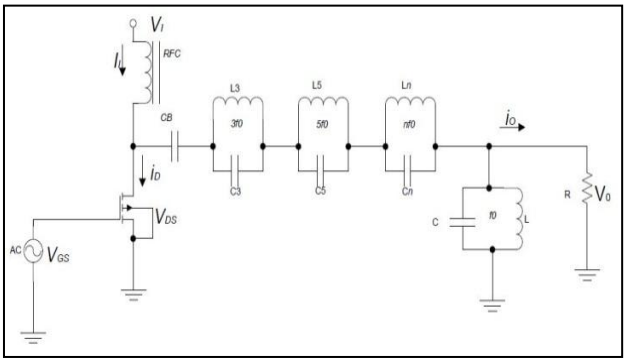

Fig 1: Ideal Class-F power amplifier

The work presented in [4] explores the analysis and design methodology for a Class-F PA in ADS software. Class-F PAs was configured using lumped elements. Maximum output power, gain and power added efficiency of 39.57dBm, 19.57 dB and 18.38% respectively were obtained by the lumped elements Class-F PA circuit at an operation frequency of 1.7 GHz, an input power of 20dBm and a bias point of V_{DS}=35 V and V_{GS}=-0.6 V.

This paper presents the design and analysis of Class F power amplifier. The Class F amplifier is used in a base station for mobile system because of its high efficiency. The result obtained shows that the Class F power amplifier can be used on a wide band spectrum, the amplifier works at 850MHz and has very good power added efficiency (PAE) and gain. The amplifier can also work at 1800MHz at input power greater than 15dBm.

2. CLASSES OF POWER AMPLIFERS

GaAs-FET PAs used in transceiver circuits exhibit varying degrees of nonlinearity, depending on its class of operation. The output current's harmonic content varies with the DC bias at the gate of the FET device, while maintaining a constant RF input signal. In certain applications, it may be desirable to have the transistor conducting for only a certain portion of the input signal.

The portion of the input RF signal for which there is an output current determines the class of operation. Discusses four classes of power amplifier operation, which are predominantly used in class-F. Fig 2. shows the typical classes based on the transistor transfer characteristics[5].

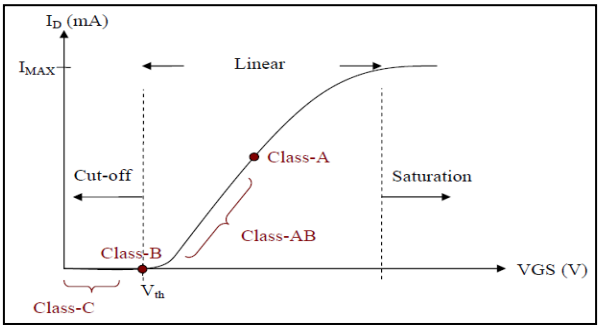

Fig 2: Classes of operation of power amplifier based on transfer characteristics

3. CLASS F POWER AMPLIFIER

Class F PA provide major improvement in PAE, output power and gain by loading the device output with appropriate terminations at fundamental and harmonic frequencies. The idea of using harmonic terminations to improve efficiency was first introduced in 1950 [6]. Basically, an amplifier can be made to operate in Class F mode by providing to the device output open-circuit terminations at the odd harmonic frequencies and short-circuit terminations at the even harmonic frequencies of the fundamental component. The resulting ideal drain voltage waveform is a square wave and the ideal drain current is a truncated sinusoid.

This results in the reduction of harmonic power since there is no flow of output current for high drain voltage and there is maximum current flow when the drain voltage waveform is at its minimum. Based on this idea, significant research has been done to determine the various factors that affect Class F performance and also the harmonic terminations required for optimum behavior.

The Class F RF PAs utilize multiple harmonic resonators in the output network to shape the drain to source voltage (V_{DS}) such that the transistor switching loss is reduced and the efficiency is increased. The drain current (I_D) flows when V_{DS} is low. V_{DS} is high when the I_D is zero. Therefore the result of I_D and V_{DS} is low by reducing the power dissipation in the transistor. In a class F amplifier with odd harmonics, the VDS contains only odd harmonics and the I_D contains only even harmonics. Therefore the input impedance of the load network represents an open circuit at odd harmonics and a short circuit at even harmonics[7]. The V_{DS} of class F amplifiers with odd harmonics is symmetrical for the lower and upper half of the cycle. The V_{DS} of odd harmonics is given by:

$$V_{DS} = V_1 - V_m \cos w_o t + \sum_{n=3,5,7,\ldots}^{\infty} V_{mn} \cos n w_o t \qquad (1)$$

The drain current I_D given by

$$i_D = I_1 - I_m \cos w_o t + \sum_{n=2,4,6,\ldots}^{\infty} I_{mn} \cos n w_o t \qquad (2)$$

4. DESIGN OF CLASS F PAs

To configure and design class-F PA, a non-linear model, FLC301XP GaAs-FET by Statz_Models was used. This model is prepared for use to operate from 0.1 to 2.5 GHz with low current, wide band and high power design[8]. Hence, 850MHz was chosen as an operation frequency.

4.1 Choice of bias point

From Fig 3. gate to source voltage (V_{GS}) was chosen (-3.8)V when drain to source voltage (V_{DS}) was chosen 4V.

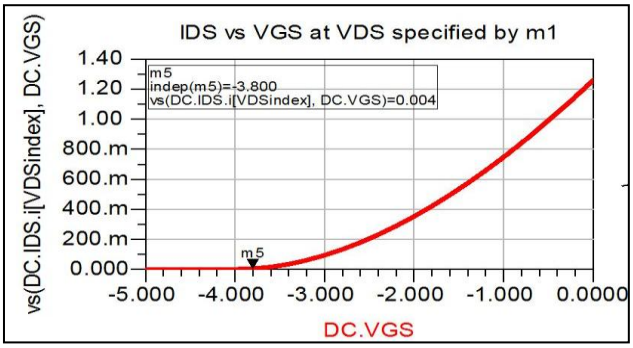

Fig 3: I_{DS} vs. V_{GS} characteristics for V_{DS}=4 V

4.2 DC-Bias Circuit Design

In lumped elements configuration, DC-block acts as an ideal capacitor used to oppose varieties in voltage while DC feed acts as an ideal inductor used to oppose varieties in current. Therefore, preventing DC current from affecting the input and output lines is done by DC block while the AC current is allowed to pass throw. DC current is allowed by DC-feed in order to bias the transistor while the AC current is blocked from passing throw[1].

4.3 Quarter Wavelength Transmission Lines

Class-F PA are usually considered as very high efficiency. Amplifiers where the high efficiency is obtained through the use of harmonic traps (L-C filters or quarter-wavelength TL) which provide suitable terminations (open or short) for the harmonics generated. Square wave drain voltage and a peaked half-sinusoidal drain current out-of-phase by 180º are produced [9]. Since only a drain voltage or a drain current exists at any given time, the power dissipation is ideally zero resulting in 100% theoretical efficiency. Fig 4. shows the structure of LPF designed at (f = 850MHz) to filtering harmonic signals out from the class-F transistor. Fig 5. represent the complete schematic design of the transistor.

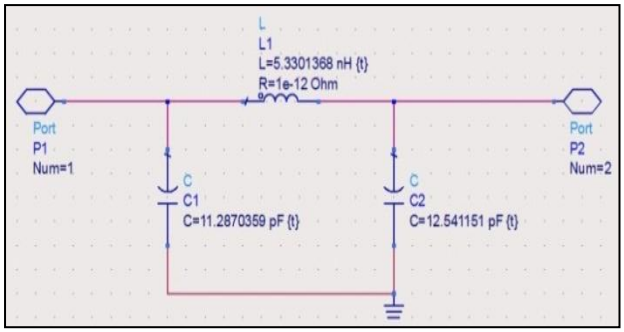

Fig 4: Schematic of Output Network for Third-Harmonic Peaking Circuit

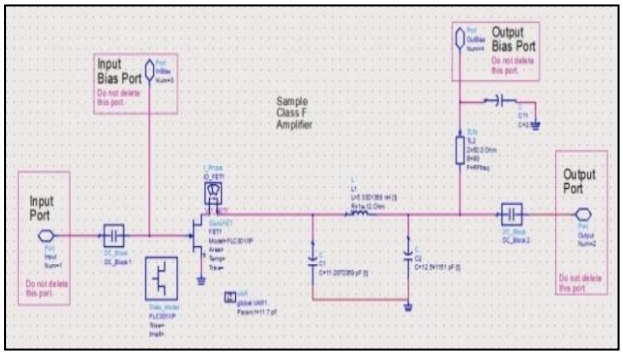

Fig 5: Schematic circuit design of class-F transistor

4.4 Active Load Pull Technique

The active load pull technique is based on the principle that applying current from a second phase coherent source can vary the resistance or reactance of a RF load. This defies the usual understanding that RF loads are physically passive entities. The analysis of the Load Pull of class-F PAs to determine load impedance for maximum efficiency as shown in Fig 6[10].

Output network was done using lumped elements. The first tank was tuned at 850MHz which is the 3rd harmonic frequency (3fo). The assumed value of C is 5.7pF and calculated value of L is 2.913nH. Fig 7. show the response of the output matching network. It can be seen that the minimum value of the reflection coefficient, -53.910 dB, occurs at 850 MHz, which means that the load is matched at that frequency.

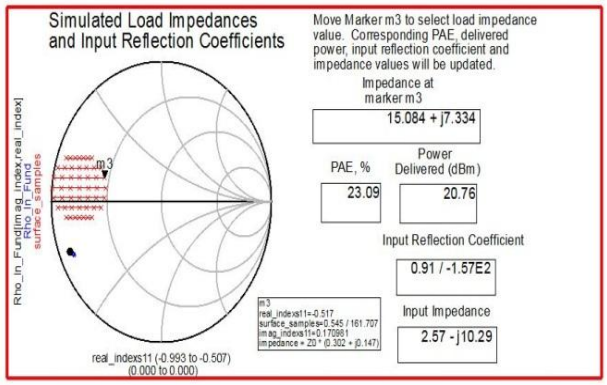

Fig 6: Load Pull Analysis to determine load impedance for maximum efficiency

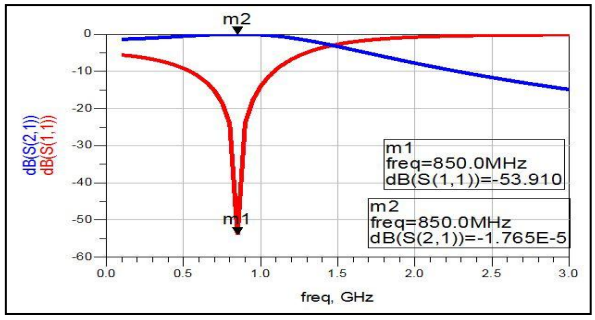

Fig 7: S-Parameters Input of the output matching Schematic

4.5 Input Matching Network

Source pull analysis to determine input impedance for maximum efficiency. It can be represent in Fig 8. Fig 9. show S-parameter output respectively. It can be seen that the minimum value of the reflection coefficient, -37.964 dB, occurs at 850MHz[10].

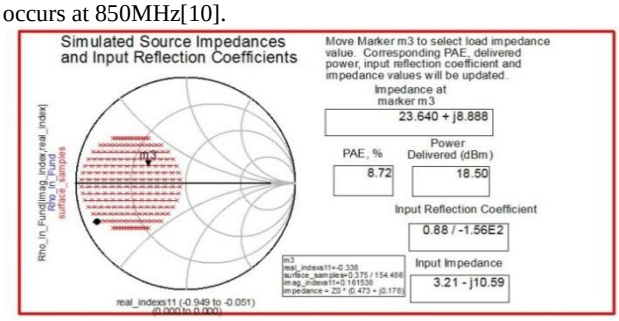

Fig 8: Source Pull Analysis to determine load impedance for maximum efficiency

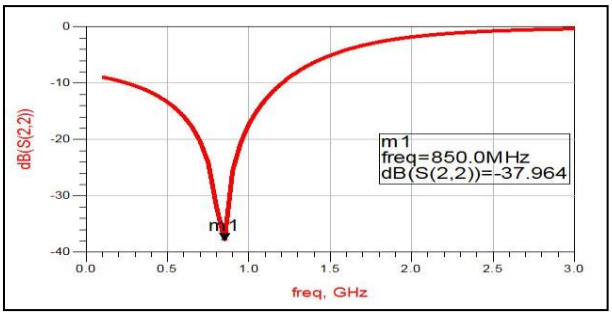

Fig 9: S-Parameters Output of the output matching Schematic

4.6 Integration Of Amplifier Components

After design and choosing operating point of the transistor amplifier, matching schematic circuits, quarter wavelength filter. We can integration of all components to design class-F power amplifier. Fig 10. explain the complete schematic circuit of amplifier at frequency 850MHz.

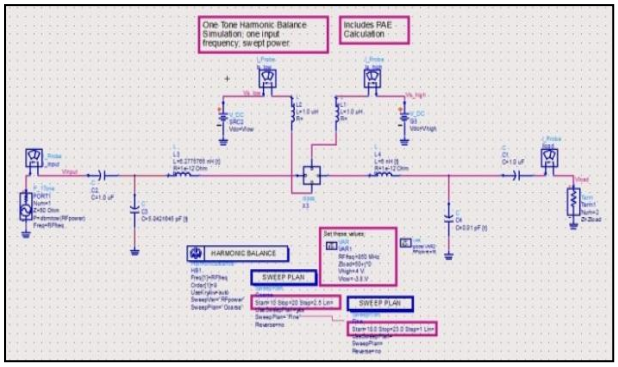

Fig 10: Schematic of the Lumped Elements Class-F PA Circuit

5. SIMULATION RESULTS

The Class-F PA has been designed in this work by using ADS software for GSM base-station. Class-F is a represent of class B stage. One tone simulations were performed with a center frequency of 850MHz. Various procedures involved in the design of power amplifier such as DC simulation, bias point selection, source, load pull characterization, matching circuit design and the design of suitable harmonic traps are explained. One-tone harmonic balance simulations were performed on the PA design. Harmonic balance is a frequency-domain analysis technique for simulating distortion in nonlinear circuits. Harmonic balance determines the spectral content of voltages and currents in the circuit. It is very useful to compute intercept point and intermodulation distortion. This is also used to determine PAE of the amplifier in the presence of interferers. The final realization of class-F PA design on the one tone simulation was explained in Fig 10.

The amplifier has good PAE% is equal to (61.22%) at 1dB maximum output power (22.31dBm) as show in Fig 11. The minimum value of amplitude and phase distortion was obtained is shown in Fig 12. Furthermore the amplifier has high linearity and low distortion, see the output spectrum at fundamental frequency on Fig 13.

Fig 14. shows a power sweep with output power, PAE, and gain as a function of input power. The characteristic behavior of the class-F power amplifier is apparent from the fact that the PAE reaches an initial peak and remains high until peak power is reached. This initial peak in PAE at (61.22%) occurs at an output power of (22.31dBm).The P1dB is at Pin,1dB (18.5dBm) and Pout,1dB (21.3dBm). at input power (20dBm).

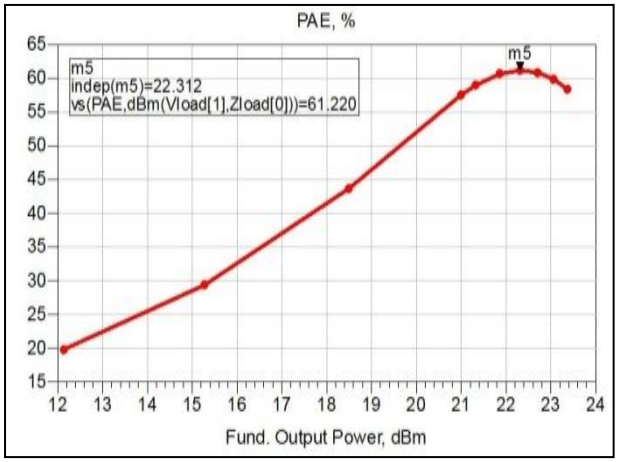

Fig 11: Power Added Efficiency (PAE%) of the class-F PA design at 1dB maximum output power.

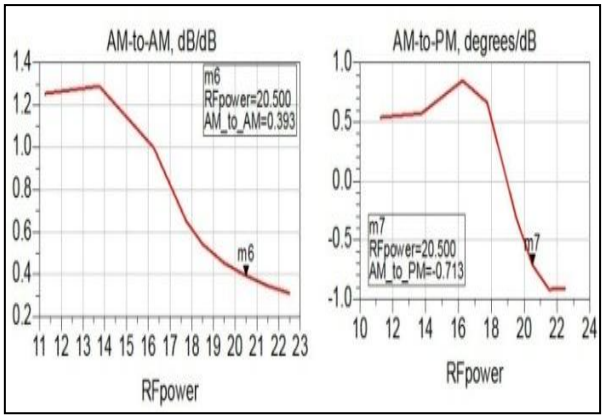

Fig 12: Amplitude distortion and Phase distortion

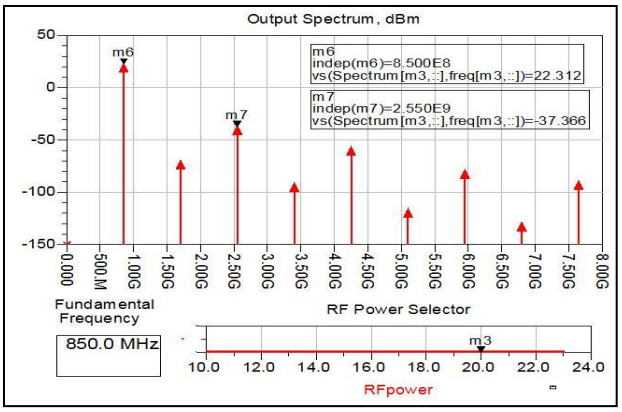

Fig 13: Output spectrum of the Class-F PAs

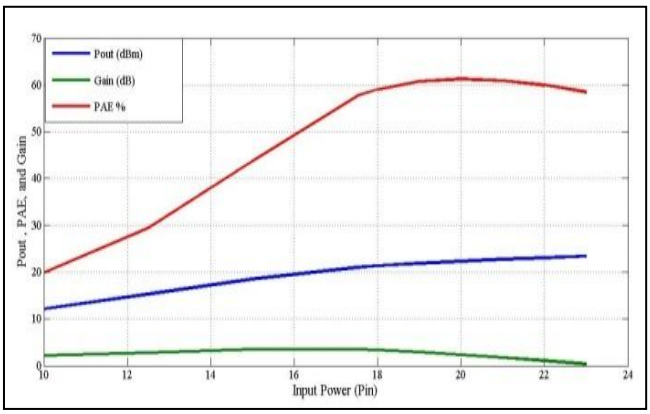

Fig 14: Output power, gain, and PAE as a function of input power

6. CONCLUSION

The analysis and design of the class-F PAs was studied at operating frequency 850MHz. It is found that the amplifier can operate at GSM base station mobile system at input power level more than 20dBm. The amplifier has good output spectrum and the 3rd harmonic spectrum is less than the main spectrum by amount of 40dBm or more. The amplifier has very good PAE, gain and output power at Pout(Max). The 3rd intermodulation (IDM3) has been obtained about (-54.32dBc) at Pout(Max) (23.36dBm), Pin (23dBm). The amplitude distortion is gotten about (0.393 dB/dB), and phase distortion about (-0.713 degree/dB).

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