Abstract

This paper represents the Nova decoder design for latest standard of video coding H.265/HEVC. Power optimization is the main priority of the propound decoder at various levels of the system like wise physical, circuit, algorithm and architecture levels. The proposed design is able to decode QCIF 30fps at maximum frequency with optimized power supply and 80% in area reduction with UMC 180nm technology. Video quality and less power dissipation is the highest priority for the portable devices in the present era in which our propound design will meet all requirements.

References

2. ke xu chiu sing choy “Priority-Based heading one detector in H.264/AVC decoding”,
5. Gary j.sullivan “overview of high efficiency video coding (HEVC)standard.1051-8215 2012 IEEE.
9. Tsu-Ming Liu, Wen-Ping Lee, Ting-An Lin and Chen-Yi Lee “A Memory-efficient Deblocking filter for h.264/avc video coding” by the National Science Council of Taiwan, R.O.C., under Grant NSC 93-2220-E-009 -010.

Index Terms

Computer Science

Circuits and Systems

Keywords

H.265/HEVC, Baseline Decoder, CAVLC / CABAC.