Abstract

This paper represents the Nova decoder design for latest standard of video coding H.265/HEVC. Power optimization is the main priority of the propound decoder at various levels of the system like wise physical, circuit, algorithm and architecture levels. The proposed design is able to decode QCIF 30fps at maximum frequency with optimized power supply and 80% in area reduction with UMC 180nm technology. Video quality and less power dissipation is the highest priority for the portable devices in the present era in which our propound design will meet all requirements.

References

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Index Terms

Computer Science    Circuits and Systems

Keywords

H.265/HEVC, Baseline Decoder, CAVLC / CABAC.