Research and Implementation a Short-Wave Transceiver System using FPGA/DSP based on SDR Technology

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ABSTRACT
In this paper, a model of radio transceiver for HF communication with Amplitude Modulation (DSBSC/SSBSC) using FPGA based on Software Defined Radio (SDR) technique is proposed. Due to the advantages of SDR technique, the transceiver can process directly and flexibly HF signal in digital domain and integrate with data processing software using standardized protocols. The results of transceiver's operational test with real-time voice signals which are analyzed based on experimental measurements demonstrate feasibility and scalability with customizable features for practical applications.

Keywords
High Frequency – HF, Amplitude Modulation – AM, FPGA, Software Defined Radio – SDR.

1. INTRODUCTION
The short-wave communication systems (HF band) perform receiving and transmitting signals through space by reflecting in the ionosphere [1][2]. Density of electrons in the ionosphere varying with the solar cycle makes altitude of layers in the ionosphere change and become the semiconductor medium. When the HF waves reach the layers, they will be bent and reflected towards the ground, and keep being reflected on it. Therefore, the waves are reflected continuously. This characteristic helps to transmit waves in the ionosphere. Due to the wave propagation properties in the ionosphere as analyzed above, HF band can be transmitted for very long distance and used in coastal communications as illustrated in Figure 1.

In recent times, the HF-SSBSC transceiver architecture has been developed on programmable hardware platform that includes a set of hardware and software parts. With this platform, the functions of the radio systems are implemented with software and hardware which can be adjusted to work on programmable process techniques. HF-SSBSC communication systems can be used to replace satellite communication systems in case of no light of sight with long distance propagation [3]. New generation HF transceivers are designed and implemented on some modern technology platforms that include FPGA, DSP, SOC and other programmable processors. The use of these technologies allows new radio features to be added to existing radio systems without requiring new hardware. SDR technique plays an important role in the development of radio receivers by enhancing flexibility with programs, meeting standard compatibility and being able to flexibly customize functionality of the system.

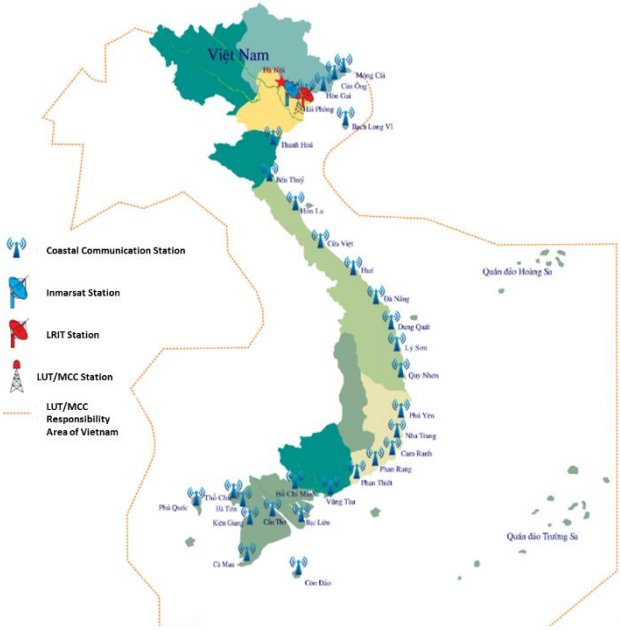

Fig 1: Map of coastal communications system in Vietnam [3]

The paper is organized as follows: Section II presents the model of short-wave transceiver system. Section III provides in detail of HF transceiver design. The experimental model and implemented results are presented in Section IV. Finally, the conclusion about the design solutions is shown in Section V.

2. HF TRANSCEIVER SYSTEM MODEL

2.1 Signal transceiver model through the Ionosphere

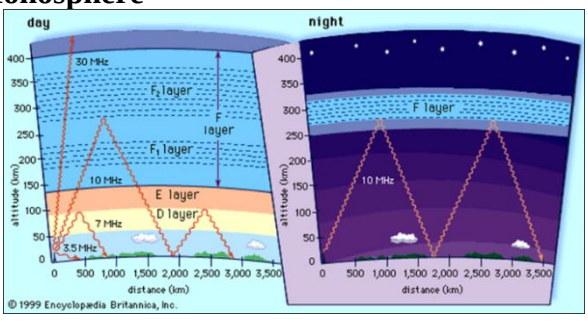

Fig 2: Propagation of shortwave/HF radio waves [4]

The band of HF signal is 3 MHz to 30 MHz which is called short-wave signal. The energy of short-wave radio frequency is capable of reaching anywhere on Earth because it can be refracted back to Earth by the ionosphere. The ionosphere is defined as the atmospheric area from altitude of 60 – 70 km to 1,000 km. The specific characteristic of the ionosphere is high conductivity because the air components are ionized by solar radiation. This fact creates an atmospheric environment that can conduct electricity, refracts the HF waves (Fig.2) and allows transmission of waves at extremely long distances.

2.2 HF Amplitude Modulation

Amplitude modulation is a modulation technique which changes the amplitude of the carrier signal according to the amplitude of the information signals. The principle of AM is the process of multiplying a baseband signal with a sinusoidal HF carrier signal. A center frequency of the generated AM signal is the carrier frequency with varied amplitude. Single-sideband (SSB) modulation can be performed in three ways: band – pass filtering, phase – shifting (Hartley method) and hybrid of two (Weaver method). The first method is shown in Fig. 3. The modulation signal $m(t)$ and carrier $V_{LO}(t)$ are fed into the balance modulation. After the balance modulation, two sidebands are obtained. By using the BPF filter, the upper or lower sideband is selected.

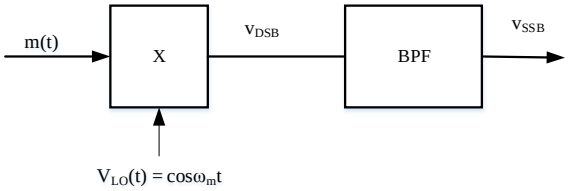

Fig 3: Generating SSB signal using band-pass filtering

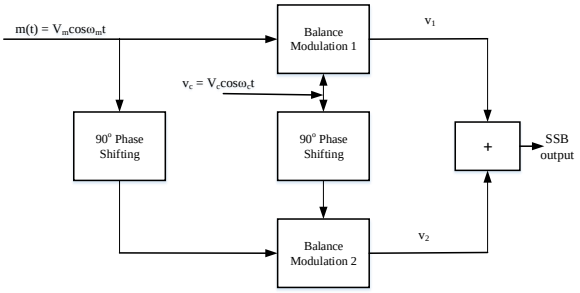

Fig 4: Generating SSB signal by Hartley method

SSB signal using Hartley method is shown in Figure 4. The input signal $m(t)$ and carrier V_c directly pass through balance modulator 1 and before passing through balance modulator 2, they are rotated 90^0. The output signal of two balance modulators passes through an adder (or a subtractor) and the output of the adder (or subtractor) is SSB signals.

The SSB signal using Weaver method is plotted in Figure 5. The output signal of balance modulator 1 is

$$V_1 = m(t)sin\omega_0 t = V_m \cos\omega_m t.sin\omega_0 t = \frac{V_m}{2}[\sin(\omega_0 + \omega_m)t + \sin(\omega_0 - \omega_m)t] \quad (1)$$

Passing the LPF1, the remaining component is $\frac{V_m}{2} sin(\omega_0 - \omega_m)t$

The output signal of balance modulator 2 is

$$V_2 = m(t)cos\omega_0 t = V_m cos\omega_m t.cos\omega_0 t = [cos(\omega_0 + \omega_m)t + cos(\omega_0 - \omega_m)t] \quad (2)$$

In case of the LPF2, the remaining component is $\frac{V_m}{2} cos(\omega_0 - \omega_m)t$

The output signal of balance modulator 3 is

$$V_3 = \sin(\omega_0 - \omega_m)\, t.sin\omega_c t = [cos(\omega_c - \omega_0 + \omega_m)t - cos(\omega_c + \omega_0 - \omega_m)t] \quad (3)$$

The output signal of balance modulator 4 is

$$V_4 = cos(\omega_0 - \omega_m)t.cos\omega_c t = [cos(\omega_c + \omega_0 - \omega_m)t + cos(\omega_c - \omega_0 + \omega_m)t] \quad (4)$$

The SSB signal is generated by adders V3 and V4:

$$V_{SSB}(t) = V_3 + V_4 = cos(\omega_c - \omega_0 + \omega_m)t \quad (5)$$

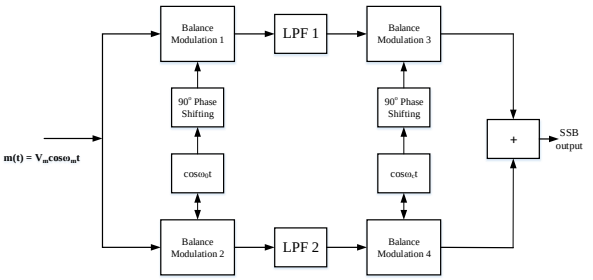

Fig 5: Generating SSB signal by Weaver method

2.3 HF transceiver model on FPGA/DSP platform

In this research, the HF transceiver system is implemented on Altera's FPGA/DSP Cyclone V SoC 5CSXFC6D6F31C6N platform [6] and SDR HackRF One platform [9]. The connection pattern between the transmitter and receiver through HF transmission channel reflected in the ionosphere is shown in Figure 6.

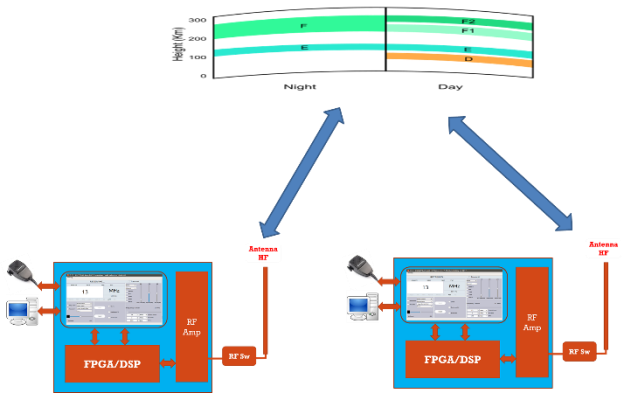

Fig 6: The functional components of the system

3. SYSTEM DESIGN

3.1 HF transmitter design on FPGA Cyclone V SoC DE10 platform

The architecture of system is given in Fig.7. In this kind of system, voice or audio signals are captured directly from a microphone or taken from a computer or other storage devices

and inserted into the built-in Audio CODEC WM8731 block on the Cyclone V System on Chip (SoC) DE10 Standard Development FPGA board [5]. After that, they are modulated with AM technique on FPGA, passed through (Digital to Analog Converter) DAC block to generate HF signals. HF signals will be fed into RF amplifier block and emitted by antenna. The modulation frequency of each channel in range from 1.6 MHz to 30 MHz is selected depending on user settings. Specific functions of blocks are as follows:

- Audio CODEC block: receives voice signals from Mic-in or Line-in ports, samples and send digital data to FPGA block for processing.
- FPGA block is the most important module. It configures and controls the operation of Audio CODEC, simultaneously receives digital data from Audio CODEC. Besides, it processes baseband data, modulates and transmits data to GPIO ports to put into the DAC902E block.
- DAC902E block [7]: receives digital data from FPGA and converts HF digital signal to analog signal before transmitted.
- PA block: performs HF signal amplification
- Antenna: emits modulated signals.

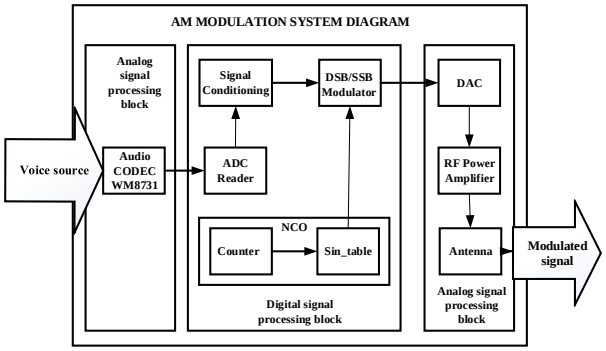

Fig 7: HF transmitter hardware architecture design

The diagram of digital signal processing block (implemented on KIT FPGA through RTL Viewer) is indicated in Fig.8. In this diagram, AudioControl block controls input/output functions of the Audio CODEC and Audio Modulation generates carrier frequency, modulates and filters harmonics before exports digital HF signal to DAC.

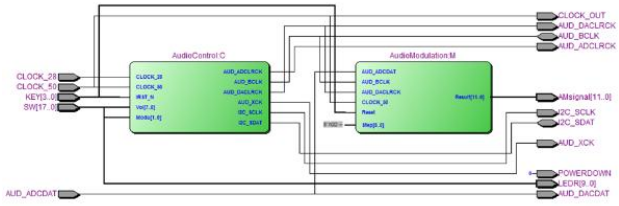

Fig 8: Block diagram of digital signal processing that is implemented on KIT FPGA

Functional blocks in AM modulation are:

- adcReader block: reads ADCDAT serial data from Audio CODEC block under the control of BCLK and ADCLRCK, then packs it into 16-bit samples.
- sine_table block: contains 512 samples of a sinusoidal signal cycle with 12 bits per sample.
- Counter block: uses CLOCK_50 for sampling sinusoidal signals. This counter has the predetermined step and this step will set the output frequency of the sinusoidal waves. For example, if the step is 128, the output frequency of sinusoidal signals will be: $f_{sine} = 50\,x\,128/512 = 12.5MHz$.
- Multiply block: performs a $12\,x\,16$ (bits) multiplier function to generate the 12-bit output as the amplitude modulated audio signals.

The principle of generating HF carrier (Fig.9): Each time the input pulse occurs; the counter block will generate a value that is passed to the input of sin_table block. Here, the value will be referenced in order to create a sample with the corresponding amplitude value of carrier. The 9-bit counter and sin_table table allow users to adjust the frequency with formula: $f = (50 \times 10^6 \times step)/512$[Hz]. The carrier frequency is adjusted by the step variable, causing the corresponding change of the time that clock pulse appears at the counter input.

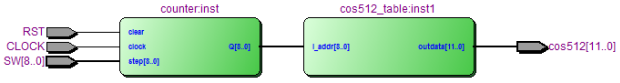

Fig 9: Block diagram of generating HF carrier

Working principle of the modulator: The adcReader block takes the digital audio/voice signals (after passing through the AudioControl) into the DSB/SSB modulator to combine with the carrier (generated from the combination of two blocks: counter and sin_table) to generate the modulated samples of HF signal according to the voice/audio signal amplitude. After that, the output will be passed through the FIR filter to filter the harmonics and then fed into the DAC block.

The DAC902E is attached to the GPIO1 port of DE10 FPGA KIT. Block diagram of DAC902E is shown in Fig.10. The input of DAC block includes 12-bit data, source and clock signals. The DAC902E output is a HF analogue signals in range of 1.6 MHz to 30 MHz.

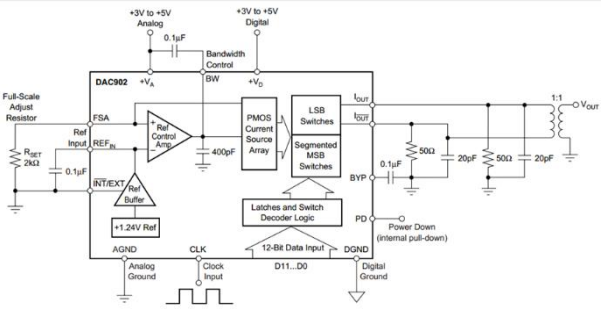

Fig 10: Functional block diagram of DAC902E [6]

A FIR filter is built on FPGA based on canonical model is shown in Fig.11. The input signal of filter (x_k) is the output bits of the AM modulator and y_k is the output bit sequences after filtering harmonics. The order of filters – N and coefficient w_j $(j = 0 \div N-1)$ is selected and designed using Matlab as illustrated in Fig.12.

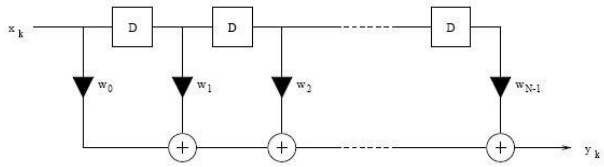

Fig 11: FIR diagram for Low Pass Filter

The HF amplifier has the frequency range, input and output power that are suitable to technical specifications. The amplifier board RFAMP-2078v308 has the schematic diagram

plotted in Fig.13. It is initiated with the parameters as follow: input power: 1 mW – 5 mW, working voltage and current in the range of 12 – 15 V and 6 – 8 A with maximum output power of 45 W and output impedance of 50 Ohms.

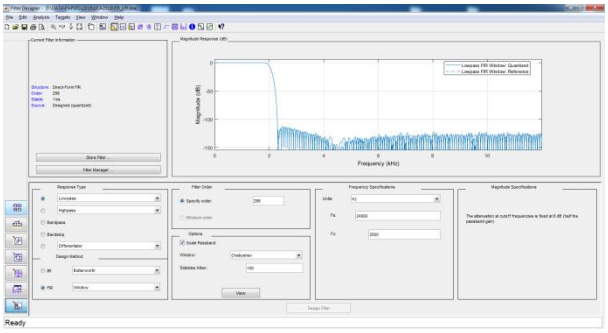

Fig 12: Matlab program interface creating filter parameters

In practice, the amplification coefficient of a HF circuit depends on some subjective factors such as the calibration of the circuit through adjusting the value of components to set the working mode of amplifier layers as well as quality of components and the capable of implementing built-in hardware.

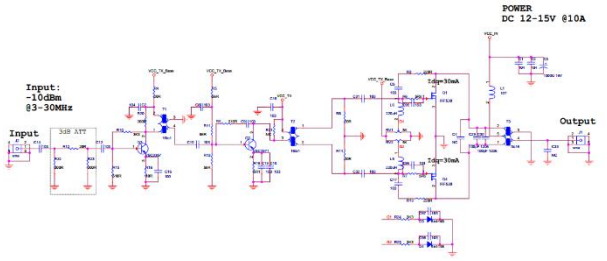

Fig 13: HF signal amplification circuit diagram

Configuration parameters of the designed HF transceiver are adjusted flexibly via a Human Machine Interface (HMI) which is implemented by QT language [7] on the Linux operating system. Data and control commands are sent from the embedded computer which installed on HPS (Hard Processor System) of Altera DE10 Development Kit to hardware part implemented on FPGA in the same board via and Advanced Extensible Interface (AXI) bridge (See Fig. 14). These data and commands are processed and interacted by HPS with FPGA components and other peripherals using inter-system connections based on UART protocol via Parallel IO controller modules in the DE10 Platform.

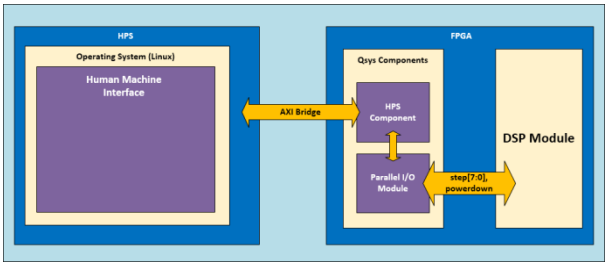

Fig 14: Connection model for controlling configuration parameters between Linux operating system based on HPS and FPGA via AXI Bridge

3.2 HF receiver design on SDR platform HackRF One

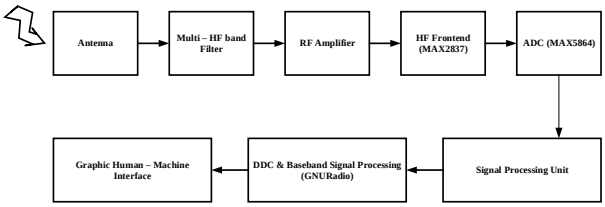

Fig 15: SDR receiver model

The HF receiver shown in Fig.16 is based on the SDR principle using HackRFOne platform [8], while baseband and IF signals are undertaken by software on PC.

In the receiver, HF signals are passed through the multi-band filter, amplifier and frontend circuit and then converted to digital domain as data bit stream which will be sent to the software on PC. The data bit stream is demodulated to obtain the original signals in order to play on the loudspeaker or store in the computer. The structure of software on HF-SDR receiver shown in Fig.16 has functions as: (1) communicates to the HF receiver using the HackRF One board to receive signals and connect to the audio reproducer, (2) processes the received signals from HackRFOne block to demodulate the AM signal recover the original signal and control audio reproduction devices or store in the computer, (3) central processing unit integrates modules in the program and connect to the Human Machine Interface module to allow users send control commands to the rest of modules.

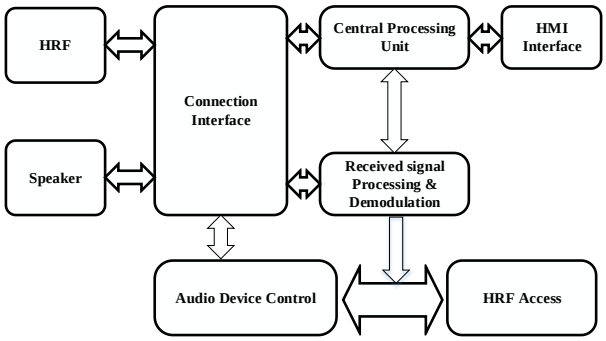

Fig 16: Software model of HF-SDR receiver

The function of HMI block is to connect to devices, receive control signals from the user and distribute setting up necessary parameters to other units in order to obtains the desired signals. The main interface can be recapitulated including the following basic blocks:

- Overview display block: shows installed parameters
- Device connection and audio settings block: display and connect HackRF, audio devices, audio-input sampling rate and audio level.

Frequency and demodulation mode settings and sensitivity block: change parameters such as center frequency, offset, modulation mode, reception channel and sensitivity of HackRF input.

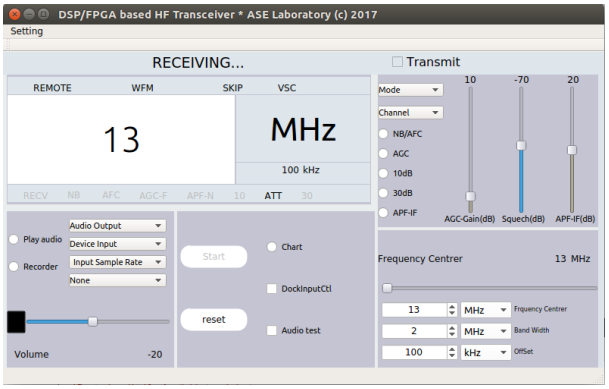

Fig 17: HF receiver interface

4. EXPERIMENTS AND EVALUATION

In this work, the proposed system is installed in two sides: transmitter and receiver.

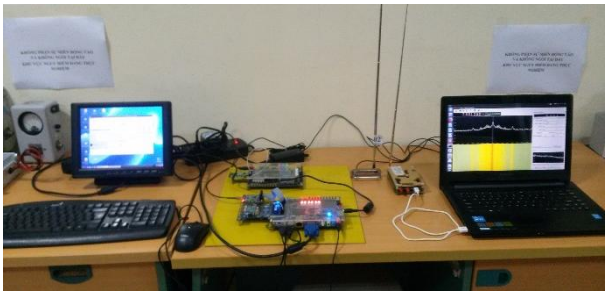

Fig 18: An experimental test case of FPGA/DSP based HF transceiver

Figure 18 shows the transmitter model including: The PC to generate information signals, FPGA board, DAC902E, HF power amplifier, transmitting antenna, source and wires. Audio data is obtained from the signal generator modules such as mp3 player or FPGA's Line-in ports. Data is sampled in Audio CODEC and fed into the FPGA chip for being modulated, then brought to the DAC902E, passed through HF amplifier and emitted by the antenna. Figure 19 shows the receiver model including receiver antenna, multi-band HF filter, HF signal amplifier, HackRF One board, embedded computer, power source and wires. The received signal from the antenna is filtered, amplified and then transferred to RFin port of HackRF One board for processing and generating a bit stream. This stream is sent to the embedded computer for IF processing and AM demodulation using GNURadio library [9]. After demodulation, reconstructed signals are delivered to a loudspeaker or saved to files for storing in the computer.

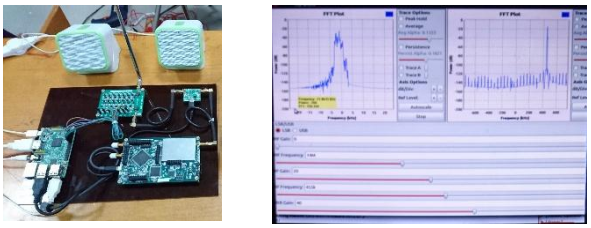

Figure 19: The model of HF-SDR receiver

Testing scenarios were performed using IFR2025 signal generator [10], R2600 communication system analyzer [11] and E5602 ENA-L radio network analyzer [12]. Aeroflex's IFR2025 signal generator has the main parameters as follow: frequency range from 9 KHz to 2.5 KHz, power from -140 dBm to +13 dBm with 0.1 dB accuracy and supports for types including AM, FM, FSK and Pulse Modulation. R2600 communication system analyzer is used to test, measure radio communication devices in the frequency range of 400 KHz to 1 GHz, this machine performs basic functions such as generating HF signals, measuring receiver sensitivity and analyzing radio spectrum. The E5062A ENA-L radio analyzer has some major functions and features such as supporting the 300 KHz to 3 GHz band, measuring S or T/R parameter integration, testing port resistance (50 or 75 Ohm), dynamic range 120 dB. Figure 20 illustrates model of a test for the HF amplifier test using signal generator IFR2025 and spectrum analysis machine R2600. Figure 21 indicates sample test for measuring the characteristic of HF antenna using E5062A ENA-L which based on three main criteria: the return loss, SWR (Standing Wave Ratio) and output impedance matching shown in Smith chart with testing bands from 300KHz to 30MHz.

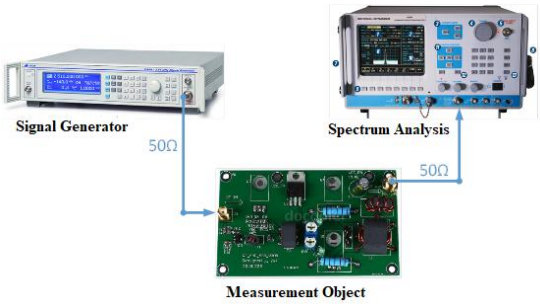

Fig 20: Model of measuring and testing HF amplifier coefficient

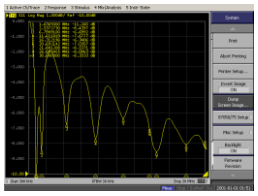

Figure 21. Measuring antenna using E5062A

Figure 22. Measuring HF signal

The results indicate that different antennas have different effective working frequencies, different output impedance with each frequency and the best impedance has the value is up to 50 Ω (in condition of impedance matching). To overcome the harmonics impaction, FIR filter at the output must be executed before signals entering DAC902E block. With this model, a 60-TAPs FIR filter is used. In case of 18066406 Hz, the obtained result reduces a background noise to -30 dB while the increases the signal power increases to 12dB in comparison with no FIR case. However, the number of selected samples when designing the filter also greatly influences measured results. By increasing the sample number of filter from 60 to 128, with a -15dB background noise, the signal power is increased approximately 27dB. Obviously, if the signal power is increased, the background noise will be also pulled up. Therefore, the sample number of filters should be selected and regulated to match standards of the transceiver system.

5. CONCLUSION

This paper presents the results of research on designing short-wave transceiver system that is implemented on modern FPGA/DSP based on SDR technique. Test results demonstrate that the proposed solution is feasible for good transceiver results in the laboratory scale. Further research will improve the model, implement field testing as well as supplement

quality assurance mechanisms for communication over the HF radio channels.

6. ACKNOWLEDGMENT

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