Design and Implementation of Digital Cheybshev Type I filter using XSG for Noise Reduction in ECG Signal

Kaustubh M. Gaikwad
Associate Professor, Department of E&Tc
Sinhgad Academy of Engineering, Kondhwa, Pune

Mahesh Chavan
Professor, Department of Electronics
KIT's College of Engineering, Kolhapur

ABSTRACT
This paper, depict the use of Chebyshev type I filter for noise reduction in ECG Signal. The filter is designed using FDA Tool of Matlab and then filter coefficients of realized filter are used for implementation of the filter on XSG. Simulation results show the filter works effectively for denoising the biomedical signal. The designed filter is efficient as per area, computational complexity and power.

General Terms
Digital Signal Processing, Biomedical signal, FPGA

Keywords
XSG, Chebyshev Filter, Noise Reduction

1. INTRODUCTION
Filters are electronic devices used to modify amplitude or phase response of a signal according to their frequency. The digital IIR filters are used for many applications. The most emerging application is IIR filters are used for the suppression of noise in ECG signal. In diagnosis of ECG signal, signal acquisition must be noise free. So the doctors are able to make correct diagnosis on the condition of heart. IIR filters can be used to remove noise present in ECG signal. Adaptive IIR filters can also be used to control active noise. IIR filters can also be used in Image Processing Applications. IIR filters can be implemented on XSG to enhance the computational speed of filters. The speed of computation is greatly increased by implementing a filter on an FPGA, rather than on a conventional DSP processor. Digital IIR filters are designed from the classical analog designs which include the following filter types:

- Butterworth filter
- Chebyshev-I filter
- Chebyshev-II filter,
- Elliptic filter.

Various researchers have worked on FPGA implementation of DSP blocks. Sunil Kumar Yadav and Rajesh Mehra have examined the optimal implementation cost performance of various IIR Filters, which are relevant for real time application therefore these filter can realize any transfer function. They have designed IIR filter and analyzed it by FDATOOL and the implementation cost has been compared on the basis of filter order, multiplier, adder, and input samples.[1]. Suvadip Roy et.al has designed a digital filter from the analog filter specifications and implemented the digital filter on a FPGA development board. The Digital Filters were designed by defining the filter specifications in the analog domain, and then transforming the analog filter specifications into digital filter specifications, defining the order of the filter, the sampling rate and type of filter to be used like a FIR or an IIR filter depending on the specifications like pass band ripple, linear phase requirement.[2] Manish Kansal et.al have designed and implemented digital filter for removal of Power supply Noise. The various blocks used in architecture of Digital IIR filter are multipliers, adders, flip flops. Generally, the recorded ECG signal is often contaminated by noise and artifacts that can be within the frequency band of interest .In order to extract useful information from the noisy ECG signals; it is required to process the raw ECG signals using digital filters. They have used MATLAB for this purpose as it is the most advanced tool for DSP applications in order to check the feasibility of the specifications in MATLAB. They have got the desired results in MATLAB. Then the filter with the desired specifications was designed in VHDL and simulated in Modelsim software.[3] Sujata Prabhakar et.al have discussed some basic theory of digital filters and then analyzed the parameters of various digital filters. They have considered the parameters such as development cost of filter, robustness, frequency response of different filters. Based on this parameters various digital filters are compared and among this chebyshev I and Elliptic filters gives good performance.[4] Kaliprasanna e.tal has demonstrated the design and implementation of Equiripple linear-phase FIR low pass filter. The filter is modeled using Simulink in XSG. The filter Coefficients are generated with the help of FDA tools, and the System Generator tool is used for RTL code generation. The design has been prototyped on Spartan-3 DSP prototype board XC3S500fg320 using Integrated Synthesis Environment (ISE) 13.1 tools all in one design suit from Xilinx.[5] Dr Manal H Jassim e.tal have implemented a digital high pass FIR filter using MATLAB program(FDA Tool) in which sampling and windowing methods are used, then the design in the FPGA kit is executed by generating VHDL description. A comparison the amount of the component has been used in the FPGA for both methods. The FIR filter is implemented using Spartan 3AN- XC3S700a-4FG484FPGA and simulated with the help of Xilinx ISE (Integrated Software Environment) Software WEBPACK Project Navigator 11i.[6] Seema rani et.al have presented the comparisons of Digital FIR &IIR filter complexity and their performances to remove Baseline noises from the ECG signal hence it is desirable to remove these noises for proper analysis and display of the ECG signal.[7] Mahesh S Chavan et.al have suggested digital filter instead of using filter using hardware for the noise removal. This paper deals with the application of the chebyshev type II for the reduction of the artifacts in the ECG Signal. The different parameters are taken under consideration such as Design procedure, its implementation to the real time ECG and the performance is depicted in the paper. Filter works satisfactorily.[8] Manish Kansal have implemented IIR filter after checking feasibility using Matlab and Modelsim. The implemented filter gives the correct pre synthesis and post-synthesis simulation results and requires less memory on FPGA kit as compared to FIR. Thus the importance of FPGA implementation considering different factors is discussed. [9]

Vladimir M Poucki et.al has proposed a filter sharpening method on the Chebyshev IIR filter and then it is implemented on FPGA.This method is attractive for filter design without extensive analysis of non-linear effects [10].

2. DIGITAL FILTER INFORMATION

The digital filter information is given below, the table 1 describes the detail information of Chebyshev type I filter used for design, table 2 shows filter specifications used during implementation of filter, and whereas table 3 shows implementation cost in terms of number of components such as multipliers and adders used.

Table 1: Chebyshev IIR Type I Filter Information

Filter structure	Direct form II
Number of sections	1
Filter Stability	Stable
Linear Phase	No
Design algorithm	Cheby1

Table 2: Filter Design Specifications

Sampling frequency Fs	1000Hz
Filter response	Low pass
Filter order	2
F_{cutoff}	0.2
3dB point	0.23984
6dB Point	0.28601
Passband Ripple	1 db

Table 3: Filter Implementation Cost

Number of Multipliers	5
Number of adders	4
Number of states	2
Multiplication per input sample	5
Addition per input sample	4

3. DESIGN SCHEME

The important information in the ECG signal lies in the frequency range of .05Hz to 100Hz.It is decided to design a low pass IIR Chebyshev type I filter of cutoff frequency 100Hz to remove high frequency noise signal. Chebyshev filter gives flat response in the pass band. Sampling frequency used in the design of filter is 1000Hz.

3.1. Realization of Filter

The figure 1 shows design of Chebyshev filter using FDA Tool whereas figure 2 shows realization model of the filter.

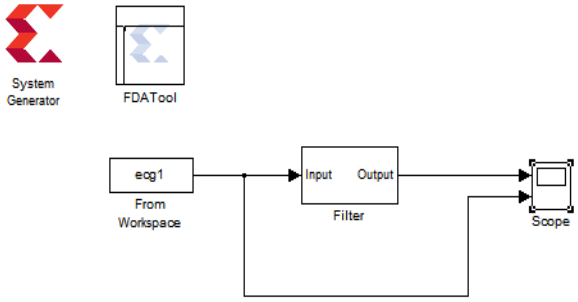

Fig. 1: Design of IIR Low pass Chebyshev filter using FDA tool

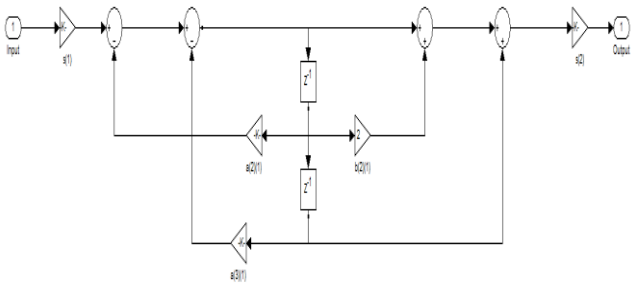

Fig. 2 : Realization model of IIR Low pass Chebyshev filter using FDA Tool.

Filter coefficients:

Numerator: 1, 2, 1
Denominator: 1, -1.1996, 0.5157
Gain: 0.0790
Output Gain: 0.8912
Transfer function:

$$H(z) = 0.08912\left[\frac{0.0769(1 + 2z^{-1} + z^{-2})}{1 - 1.1996z^{-1} + 0.5157z^{-2}}\right]$$

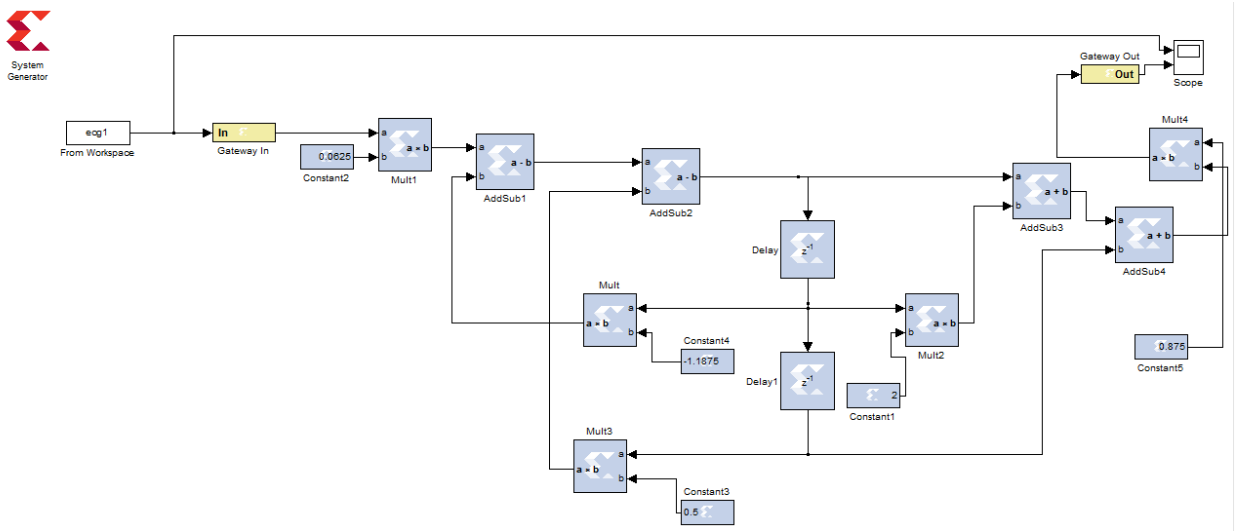

Fig. 3: Realization Model of IIR Chebyshev I Filter Using Xilinx System Generator

4. FILTER RESPONSES

The various responses are depicted in figure 4 to figure 11. These response shows that designed filter having flat response in pass band and is stable with nonlinear characteristics.

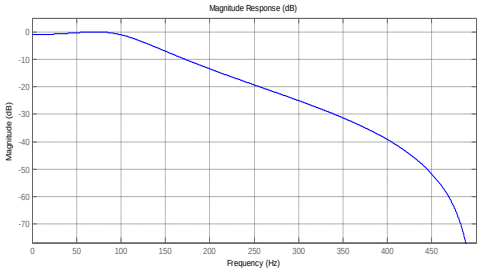

Fig.4: Magnitude Response

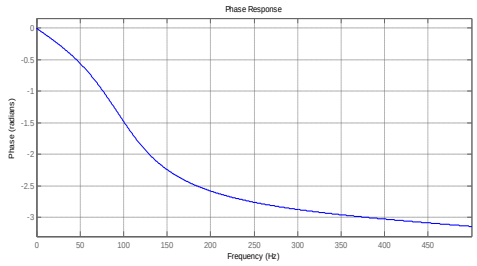

Fig.4a: Phase Response

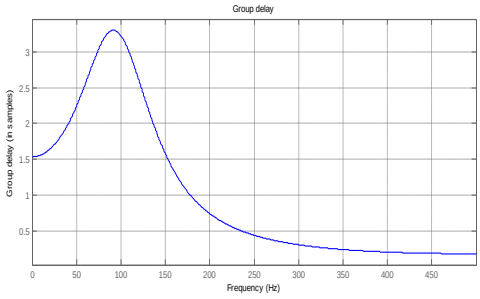

Fig.4b: Group delay Response

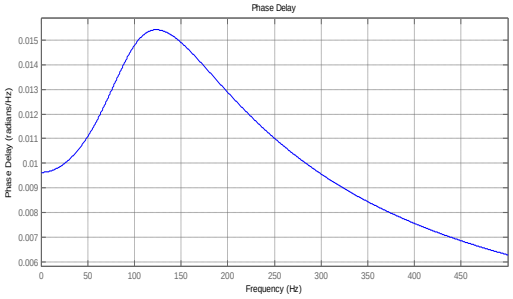

Fig.4c: Phase Delay

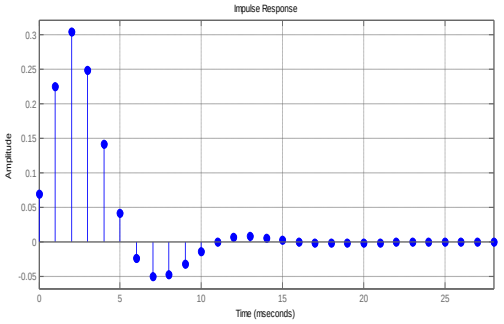

Fig.4d: Impulse Response

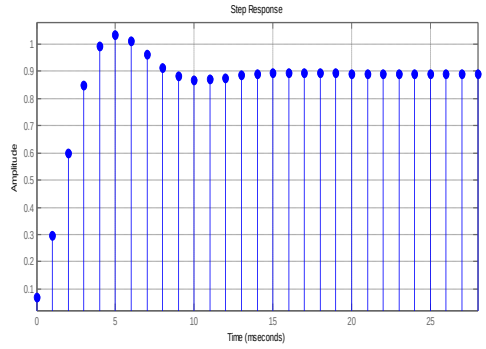

Fig.4e: Step Response

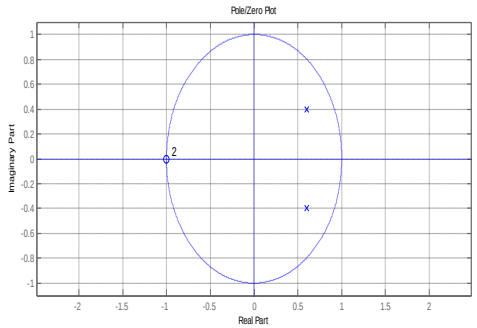

Fig.4f: Pole Zero Plot

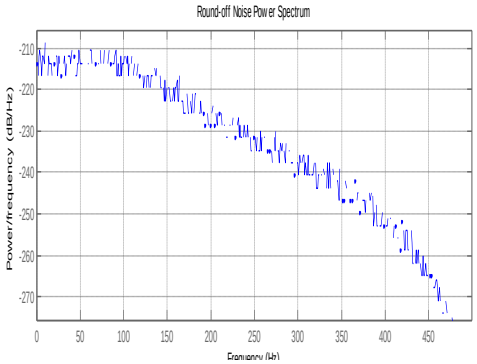

Fig.4g: Round off Noise Power Spectrum

5. IMPLEMENTATION RESULTS

The filter input and output results are shown in the figure given below which indicates input and output waveform before and after filtration.

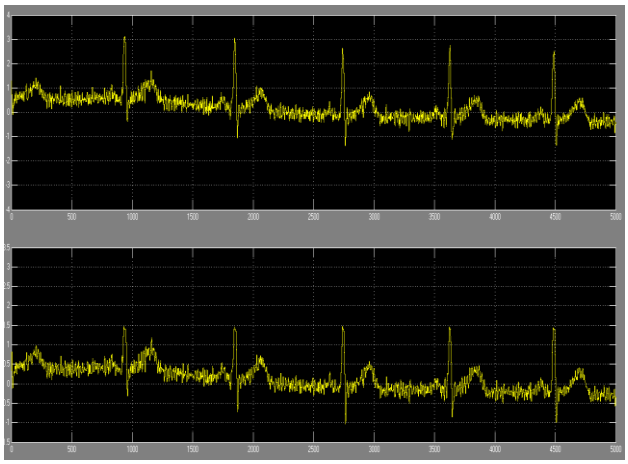

Fig.5: Input & Output Waveforms of Chebyshev I filter

5.1. Device Utilization Summary

The device utilization summary of the filter designed and implemented is given in the tabular form which specifies various aspects required for the filter implementation.

Table 4: Device Utilization Summary

Target Device	3s500efg320-4		
Product Version	ISE 14.2		
Logic Utilization	**Available**	**Used**	**Utilization**
Number of Slice Flip Flops	40	9,312	1%
Number of 4 input LUTs	240	9,312	2%
Number of occupied Slices	161	4,656	3%
Number of Slices containing only related logic	161	161	100%
Number of Slices containing unrelated logic	0	161	0%
Total Number of 4 input LUTs	262	9,312	2%
Number used as logic	240		
Number used as a route-thru	22		
Number of bonded IOBs	49	232	21%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	2.38		

5.2. Time & Power Analysis

The filter time and power analysis details are given in the table 5 which shows utilization of various parameters such as onchip clocks, signals,logic, IOs etc

Table 5: Time & Power Analysis details

0n –chip	**Power (W)**	**Used**	**Available**	**Utilization (%)**
Clocks	0.002	1		
Logic	0.005	262	9312	3
Signals	0.006	369		
IOs	0.133	49	232	21
Leakage	0.083			
Total	0.229			

5.3. RTL Schematic

The figure 6 shows RTL schematic of the filter when implemented using XSG.

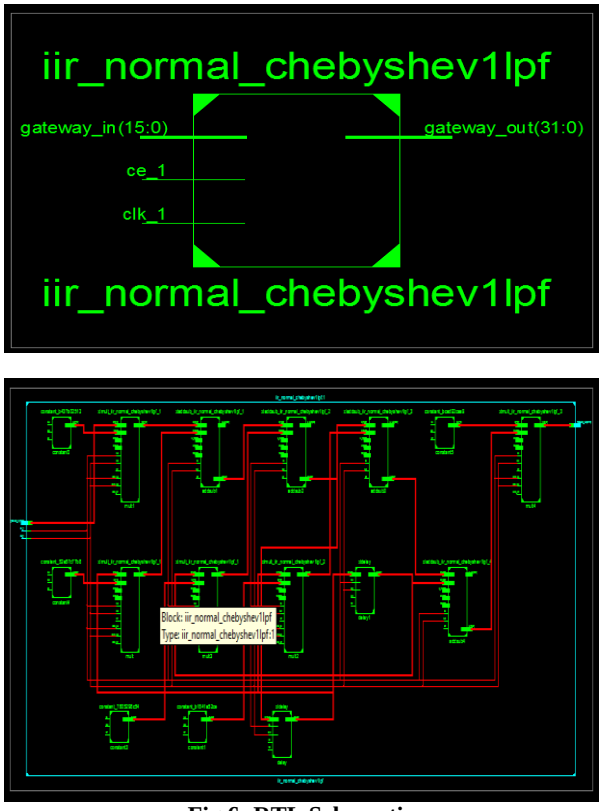

Fig.6: RTL Schematic

6. CONCLUSION

In this paper low pass Chebyshev type I filter is designed and implemented using XSG platform for processing the ECG Signal. Filter is implemented for order 2. Filter has shown good performance in terms of various parameters like area, power and Speed when used on FPGA platform. Filters detail device utilization summary, time and power analysis is depicted in the paper where it can be observed that it gives good performance which helps to remove noise from ECG Signal. It can be used for various biomedical applications using various FIR filters which can be a good future scope.

7. REFERENCES

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