Abstract

In this paper, a novel approach at circuit level named LSP is proposed by combination of LECTOR, Stack and Pass transistors techniques to decrease leakage power dissipation during active and standby mode. As a result, pass transistors are utilized to maintain logic state of network in the standby mode. Proposed technique simulation has been performed using HSPICE software in 32 nanometer technology with supply voltage 0.6V. According to achieved results by NAND gate and full adder circuits, sub-threshold current is decreased by 80% in compared to base case, 70% to LECTOR and 20% to Sleepy Keeper.

References

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Index Terms

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Keywords

Leakage power, LECTOR technique, Low power, Stack technique, VLSI.