Novel Low Leakage Power Technique of LSP in 32 nm VLSI Circuits

Adel Alimoradi
Department of Electrical Engineering
Faculty of engineering, Razi University
Kermanshah, Iran

Pourya Rostami Gooran
Department of Electrical Engineering
Kermanshah Branch, Islamic Azad University
Kermanshah, Iran

Manoocheher Karami
Department of Electrical Engineering
Shahid Rajaee Teacher Training University
Tehran, Iran

ABSTRACT
In this paper, a novel approach at circuit level named LSP is proposed by combination of LECTOR, Stack and Pass transistors techniques to decrease leakage power dissipation during active and standby mode. As a result, pass transistors are utilized to maintain logic state of network in the standby mode. Proposed technique simulation has been performed using HSPICE software in 32 nanometer technology with supply voltage 0.6V. According to achieved results by NAND gate and full adder circuits, sub-threshold current is decreased by 80% in compared to base case, 70% to LECTOR and 20% to Sleepy Keeper.

General Terms
HSPICE simulator full adder circuit, NAND gate, Nanometer technology, Power supply, VLSI.

Keywords
Leakage power, LECTOR technique, Low power, Stack technique, VLSI.

1. INTRODUCTION
Nowadays sub-threshold current reduction and control of power dissipation in high performance digital designs are as the main challenges in VLSI systems, especially for CMOS technology lower than 65nm. Therefore, Dynamic and leakage power are two important sources of power dissipation [1-5].

The dynamic (switching) power consumption occurs due to the change in the input signal, caused by charging and discharging of the node capacitance [1], [5].

Leakage power consumption is consumed when a turned-off transistor leaks current. This is called static power dissipation that has become a significant portion of total power consumption in deep sub-micron technology like 65nm and below [1], [5].

Leakage power dissipation comprises many sources component. Sub-threshold current as a main contributor of leakage is caused by a current that flows from drain to source of transistor when gate voltage is below the threshold voltage. This component of leakage power has been expressed by [6].

$$I_{DS} = I_0 e^{\frac{VGS-VTH}{nVT}}\left[1 - e^{\frac{V_{DS}}{VT}}\right] \quad (1)$$

where $V_T = V_{T0} - \eta V_{DS} + \gamma[(\phi_S + V_{SB})^{0.5} - \phi_S{}^{0.5}]$

$$I_0 = \mu_0 C_{OX} \frac{W}{L} V_{th}^2 e^{1.8} \quad (2)$$

In Equations (1, 2), I_0 is current at threshold (dependent on process and device geometry), V_{T0}, the zero bias threshold voltage; γ, the linearized body effect coefficient; n, the sub-threshold swing coefficient; V_T, thermal voltage; η, drain-induced barrier lowering effect [6-10].

Regarding the relationship between square of supply voltage with dynamic power and linear with leakage power, reducing the supply voltage is an effective way to achieve low power but without lowering threshold voltage results in drastic degradation in speed according to [10].

$$T_d = \frac{CL \times VDD}{(VDD - VTH)^{\alpha}} \quad (3)$$

Where α is positive constant channel effects about 1.3 for short channel and 2 for long channel devices. C_L is the total load capacitance.

Reducing threshold voltage as a main idea to overcome delay on one hand and scaling down feature size as rapid progress technology in semiconductor on the other hand, causes an exponential increase in sub-threshold leakage power, so that it has become a dominant portion of total power consumption [9], [10].

MTCMOS technique as one of the most well-known techniques (Figure 1(a)), isolates network from power supply and ground by using high threshold voltage switch transistors [11-14].

In [11] MTCMOS suffers from both fabrication process complex due to different threshold voltage of switch transistors from network and loss of logic state during standby mode, but proposed technique exploits low threshold voltage transistors in the whole network and keeper transistors to save logic state of circuit.

Forced Stack as another approach replaces any transistor of network by two half size transistors, as shown in Figure 1(b). This technique exploits the dependence of I_{sub} on the source terminal voltage. Simultaneous turning off of the two divided transistors induces reverse bias between them [15-18].

Problems with [15-18] are the growing number of transistors due to stacking effect resulting in large area and delay significantly, but proposed technique uses stacked transistors in very small part of network i.e. LECTOR cell, which is shown in Figure 2(a).

Technique is shown in Figure 2(a), which the source of each transistor is controlled by source terminal of the other, is known as LECTOR.

The basic idea behind LECTOR approach is that a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path [19-21].

Another important technique (named Sleepy Keeper), depicted in Figure 2(b), can reduce leakage power like MTCMOS and exploits keeper transistors in parallel to pull up and pull down switch transistors making a feedback with output to retain logic state circuit in standby mode [21], [22].

It is well- known that passing VDD with NMOS transistors and GND with PMOS transistors are not efficient which results in low swing output and delay [21], but pass transistors as logic state keepers have solved this problem in proposed technique.

This paper is organized into two main sections. In the first section, the proposed technique has been described, and simulation results has been presented, in next section.

2. POROPOSED DESIGN

LSP technique as low leakage novel circuit level technique has been depicted in Figure 3. The main construction of proposed design is based on the combination of LECTOR, STACK, with pass transistors as keepers.

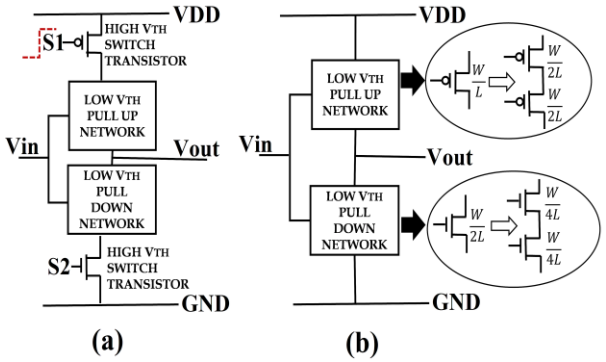

Fig 1: (a) MTCMOS technique (b) Forced Stack technique

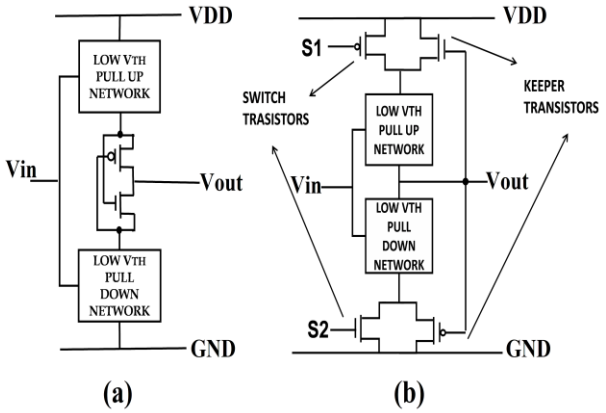

Fig 2: (a) LECTOR technique (b) Sleepy Keeper technique

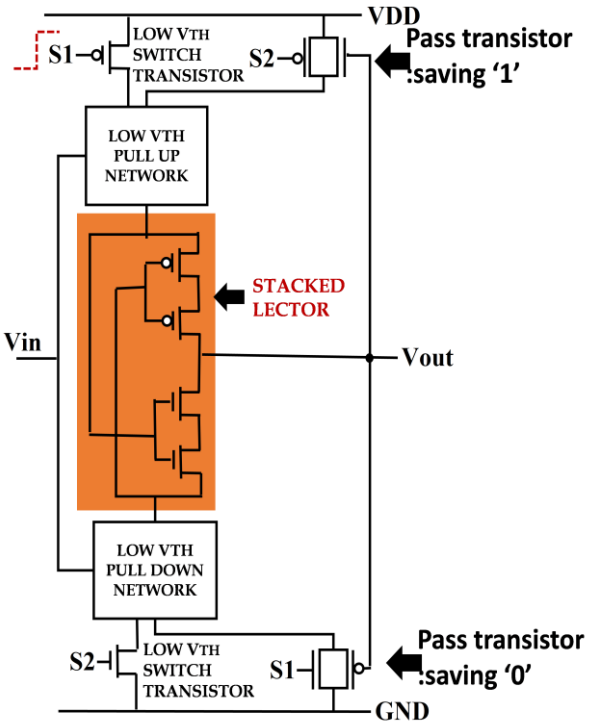

Fig 3: Proposed technique (Lector-Stack-Pass (LSP))

The significant points of this technique are not only reducing sub-threshold current, but also exploiting fewer transistors as compared to other techniques [15], [21], which decreases the fabrication cost. Since LECTOR network operates independently from status variation of inputs, it does not pay a penalty in form of switching power (dynamic power) dissipation. To improve and better control the operation of LECTOR technique, its transistors have been divided in two parts by using stack approach. Due to high resistance from supply power to output, regarding near cut off operation of LECTOR transistors, incorporating of LECTOR and Stack methods has lowered sub-threshold current noticeably (almost 3x) compared to LECTOR.

Stacked transistors of LECTOR network instead of whole circuits result in lower propagation delay and improving network operation.

Proposed design provides proper leakage power reduction in both standby and active mode, which retains the state of the circuit during the standby mode by using pass transistors with the least delay concerning the designing in 32nm technology. The method will be explained in each mode operation as below.

According to Figure 3 by asserting (S1=1, S2=0), during standby mode both pairs of P and N switch transistors are off hence network is isolated from power and GND. Since NMOS transistors are not efficient at passing PMOS and VDD transistors at passing GND, in this design, pass transistors parallel with switch transistors have been used in order to retain the state of the circuit. To save value of '1' pull up pass transistor in parallel to NMOS switch transistor is the only source of VDD to the pull-up network likewise pull down pass transistor in parallel to PMOS switch transistor maintains value '0'.

During active mode operation (S1=0, S2=1) switch and pass transistors are On. This structure can potentially improve

circuit delay since very low resistance path is established between VDD and ground to output. In addition, Stacked LECTOR between pull up and pull down network controls leakage power significantly.

3. SIMULATION AND RESULTS

Simulation processes have been performed using HSPICE software in 32 nanometer (nm) with BSIM4 model of Berkeley Predictive Technology Model (BPTM) parameters for the technologies standard CMOS at room temperature with supply voltage 0.6 V to estimate power consumption. To better understand LSP technique NAND gate depicted in Figure 4.

In order to compare proposed technique with the base case and other techniques: Forced stack, LECTOR, Sleepy Keeper, NAND gate and 1-bit full adder circuits have been chosen. Simulation results for NAND and Full Adder cases have been measured with a random input vector changing every clock cycle. The results of simulation have been explained in form of Figures 5–8. The status of the transistors NAND gate based on proposed technique, has tabulated in Table 1.

According to simulation results represented in graphs and regarding to the used number of transistors, significant decrease in sub-threshold current, approximately 2 to 4 times in both NAND and Full Adder circuits, has been achieved, compared to traditional and other designs. There is an acceptable propagation delay compared to base case concerning high resistance path LECTOR network and also slight difference in dynamic power. Figure 9 shows the output results of the Full Adder circuit according to HSPICE software. Inputs of Full Adder have been adjusted so that they can change status in different logic levels (0, 1). The outputs of circuits (sum, carry) without pass transistors have been shown according to inputs (Ain, Bin, and Cin) in part (b) and part (c) shown the effect of using pass transistors, which has caused a considerable decrease in propagation delay.

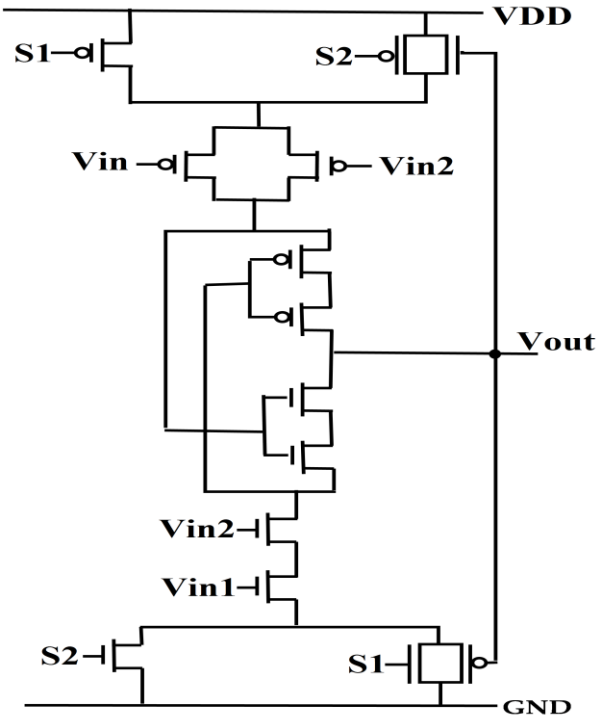

Fig 4: Proposed technique by NAND gate

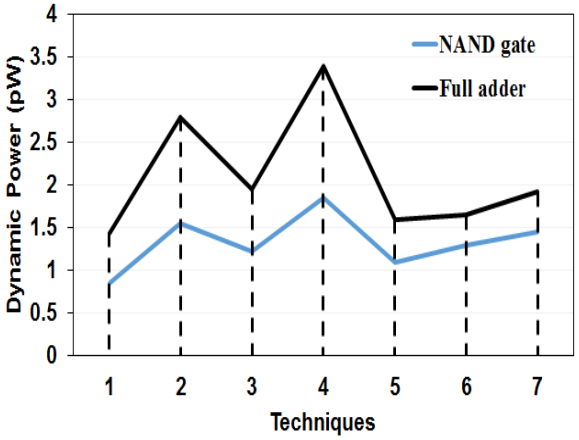

Fig 5: Shows comparing between 7 techniques for dynamic Power by NAND gate and full adder, (1) basic case (2) Force-stack (3) Force-stack-switch (4) sleepy keeper (5) LECTOR (6) LECTOR-Stack (7) LECTOR-Stack Pass

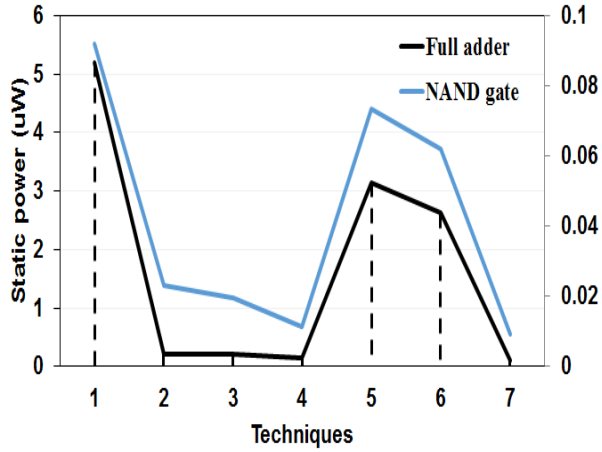

Fig 6: Shows comparing between 7 techniques for static power by NAND gate and full adder, (1) basic case (2) Force-stack (3) Force-stack-switch (4) sleepy keeper (5) LECTOR (6) LECTOR-Stack (7) LECTOR-Stack Pass

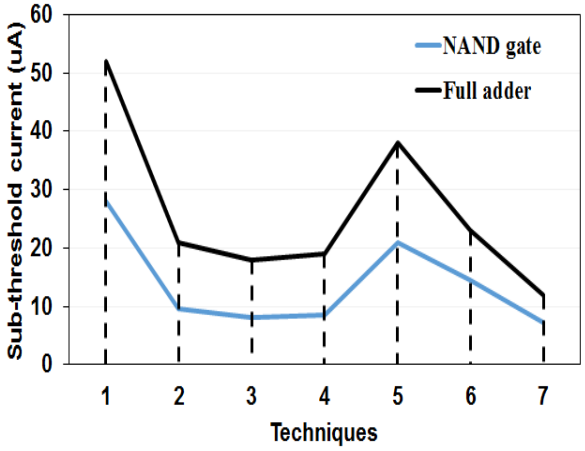

Fig 7: Shows comparing between 7 techniques for sub-threshold current by NAND gate and full adder, (1) basic case (2) Force-stack (3) Force-stack-switch (4) sleepy keeper (5) LECTOR (6) LECTOR-Stack (7) LECTOR-Stack Pass

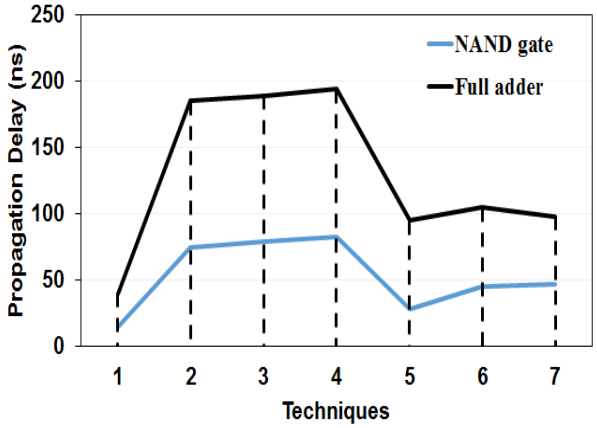

Fig 8: Shows comparing between 7 techniques for propagation delay by NAND gate and full adder, (1) basic case (2) Force-stack (3) Force-stack-switch (4) sleepy keeper (5) LECTOR (6) LECTOR-Stack (7) LECTOR-Stack Pass

Table 1. LSP NAND state matrix design

Transistors	Inputs (Ain, Bin)			
	(0,0)	(0,1)	(1,0)	(1,1)
M1	On	On	Off	Off
M2	On	Off	On	Off
M3	Off	Off	On	On
M4	Off	On	Off	On
M5	near Cut-Off	near Cut-Off	near Cut-Off	On
M6	near Cut-Off	near Cut-Off	near Cut-Off	On
M7	On	On	On	near Cut-Off
M8	On	On	On	near Cut-Off

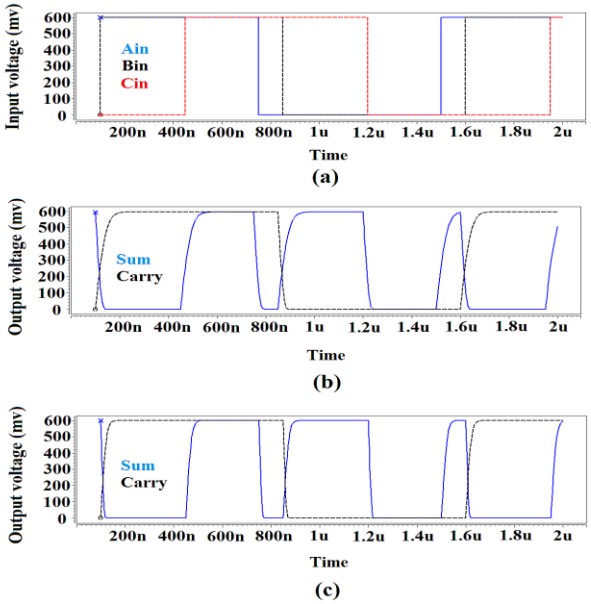

Fig 9. Inputs and outputs of the full Adder circuit, (a) Inputs Part (b) without pass transistors (c) using pass transistors

4. CONCLUSION & FUTURE WORK

In this paper LSP technique was presented as a more efficient method by NAND and full adder circuits in 32 nm technology with 0.6V power supply. Based on results LSP in compared to other approaches such as MTCMOS, LECTOR and Forced STACK had better operation in reduction leakage power. Therefore, sub-threshold current has been reduced by 80% in relation to base case, 70% to LECTOR and 20% to Sleepy Keeper. Also propagation delay has been improved, so that this technique is suitable for high speed circuits in DSM regime. In future, LSP technique as one of combined designs will be implemented in the field of VLSI systems to improve consumption power and sizing of integrated circuits.

5. REFERENCES

[1] N. Jayakumar, S. Paul, R. Garg, K. Gulati, and S. P. Khatri, "Minimizing and exploiting leakage in VLSI design," Springer, 2010.

[2] P. Kumar, and R. K. Sharma, "Low voltage high performance hybrid full adder," Engineering Science and Technology, an International Journal, Vol. 19, pp. 559–565, March, 2016.

[3] R. Taco, I. Levi, M. Lanuzza, and A. Fish, "Low voltage logic circuits exploiting gate level dynamic body biasing in 28 nm UTBB FD–SOI," Science direct. Solid-State Electronics, Vol. 117, pp. 185–192, March, 2016.

[4] A. Wang, B. H. Calhoun, and A. P. Chandrakasan, "Sub–threshold design for ultra–low–power systems," Springer. 2006.

[5] V. L. Rani, and M. M. Latha, "pass transistor–based pull–up/pull–down insertion technique for leakage power optimization in CMOS VLSI circuits," springer, Circuits, Systems, and Signal Processing., Vol. 35, pp. 4139–4152, Nov. 2016.

[6] V. K. Sharma, M. Pattanaik, and B. Raj, "INDEP approach for leakage reduction in nanoscale CMOS circuits," Tylor and Francis. International Journal of Electronics. Vol. 102, pp. 200–215, Jan. 2014.

[7] J. Seomun, I. Shin, and Y. Shin, "Synthesis of active–mode power gating circuits," IEEE Tran. Vol. 31, pp. 391–403, March, 2012.

[8] M. Kavitha, and T. Govindaraj, "Low–power multimodal switch for leakage reduction and stability improvement in SRAM cell," Arabian Journal for Science and Engineering, Vol. 41, pp. 2945–2955, Aug. 2016.

[9] P. Saini, and R. Mehra, "Leakage power reduction in CMOS VLSI circuits," IJCA Journal, International Journal of Computer Applications., Vol. 55, pp. 42–48, 2012.

[10] S. D. Pable, and M. Hasan, "Ultra–low–power signaling challenges for subthreshold global interconnects," Elsevier Integration, the VLSI journal, Vol. 45, pp. 186–196, March. 2012.

[11] A. Handa, J. Chawla, and G. Sharma, "A novel high performance low power CMOS NOR gate using voltage scaling and MTCMOS technique," In IEEE Int Conf on Advances in Computing, Communications and Informatics (ICACCI), pp. 624–629, 2014.

[12] M. Seok, S. Hanson, et al, "Sleep mode analysis and optimization with minimal-sized power gating switch for ultra-low operation," IEEE Tran on Very Large Scale

Integration (VLSI) Systems., Vol. 20, pp. 605–615, April. 2012.

[13] R. Anjana, and A. K. Somkuwar, "Optimal solution of model reduction problem," International Conference on (ICEVENT), Apr. 2013.

[14] J. N. Mistry, et al, "Active mode subclock power gating," IEEE Tran on Very Large Scale Integration (VLSI) Systems., Vol. 22, pp. 1898–1908, Sep. 2013.

[15] V. Neema, S. S. Chouhan, and S. Tokekar, "novel circuit technique for reduction of leakage current in series/parallel PMOS/NMOS transistors Stack," Tylor and Francis. IETE Journal of Research, Vol. 56, pp. 362–366, Sep. 2013.

[16] D. Baccarin, D. Esseni, and M. Alioto, "Mixed FBB/RBB: a novel low-leakage technique for FINFET Forced Stacks," IEEE Tran on Very Large Scale Integration (VLSI) Systems., Vol. 20, pp. 1467–1472, Jun. 2012.

[17] T. G. Reddy, and K. Suganthi, "Super stack technique to reduce leakage power for sub 0.5-v supply voltage in VLSI circuits," In IET International Conference on Sustainable Energy and Intelligent System., pp. 585–588, Feb. 2011.

[18] M. Sethi, et al, "A Novel High Performance Dual Threshold Voltage Domino Logic Employing Stacked Transistors," International Journal of Computer Applications., Vol. 77, pp. 30–35, 2013.

[19] A. P. Shah, V. Neema, and S. Daulatabad, "Effect of process, voltage and temperature (PVT) variations in LECTOR-B (leakage reduction technique) at 70 nm technology node," In IEEE International Conference on Computer, Communication and Control, pp. 1–6, June. 2015.

[20] T. K. Gupta, and K. Khare, "Lector with footed-diode inverter: a technique for leakage reduction in domino circuits," Circuits System Signal Process., Vol. 32, pp. 2707–2722, June. 2013.

[21] R. Lorenzo, and S. Chaudhury, "Review of circuit level leakage minimization techniques in CMOS VLSI circuits," IETE Technical Review., Vol. 33, pp. 1–23, Apr. 2016.

[22] K. N. Bhargav, A. Suresh, and G. Saini, "Stacked Keeper with body bias: a new approach to reduce leakage power for low power VLSI design," IEEE International Conference on Advanced Communication Control and Computing Teclmologies (ICACCCT), pp. 445–450, Jan. 2014.