Abstract

As semiconductor technology scaling approaches its limits, 3-D integrated circuits (3-D ICs) have been proposed as one solution to continue the push towards increasing transistor counts in VLSI circuits. Recent progress in the fabrication of three-dimensional (3-D) integrated circuits has opened the possibility of exploiting this technology to alleviate performance and power related issues raised by interconnects in advanced nanometer CMOS VLSI circuits. Physical synthesis for 3-D integrated circuits is substantially different from traditional planar integrated circuits due to the presence of additional constraints of placing circuit modules in multiple silicon layers. To realize the full potential offered by 3-D integrated circuits, high-level synthesis of these circuits must take layout-related issues unique to 3-D technology into account during the synthesis process. This paper presents a 3-D layout-aware timing-driven binding algorithm for design-space exploration during high-level synthesis. The algorithm tightly integrates the synthesis tasks of resource binding, assignment of modules to multiple silicon die, 3-D floorplanning, and through-silicon via (TSV) minimization. Elmore delay models incorporating distributed wire-delays, together with delays introduced by pins and TSVs in a 3-D integrated
circuit are used to compute data-transfer delays in a data path. Accurate estimates of individual net delays, obtained from net topologies in 3-D floorplans, are used to compute wire delays. Our experimental results show that a timing-driven binding algorithm for high-level synthesis can improve delays by an average of 12.2% and a maximum of up to 20.65%.

References


**Index Terms**

Computer Science

Algorithms

**Keywords**

High-Level Synthesis;; Three-dimensional Integrated Circuits; Simulated Annealing; Timing-driven Synthesis;