Abstract

Artificial Neural Networks (ANNs) are highly parallel and interconnected under a single layer management system. Massive parallelism, distributed representation and computation and adaptability are the most typical characteristics of ANNs. Implemented ANN on Field Programmable Gate Array (FPGA) can be used for a variety of real life applications. FPGAs are more attractive devices for its reconfigurable architecture and lower power consumption than other processors. The lower non-recurring engineering (NRE) costs and short time to market for FPGAs are making it highly demand in hardware implementations. This paper proposes implementation of ANN architecture with feedforward network topology. To improve the speed of the system a LUT based activation function is implemented as a ROM which contains neuron synaptic weights and thus stores the inner product. The design has been synthesized and implemented on a Xilinx Spartan 6 target device using 14.7 ISE Design Suite and results are discussed. Design implementation of this proposed architecture is being enhance the overall performance of the system and as well as saving the area. The computation execution time of
the proposed ANN architecture is 643.977 MHz which leads to fastest operation.

References

Index Terms

Computer Science

Artificial Intelligence

Keywords

ANNs, FPGA, LUT, Neural Network; VHDL