This paper proposes a modified form of the design for low dynamic power adder using a reset network in the CMOS dynamic logic family. The results show that the dynamic power reduces as compared to lower dynamic power logic and the domino logic. In this modified form of the low dynamic power adder, the logic outputs are reset to low during the pre-discharge phase.
which is the high input to the clock. The logic evaluation takes place when the clock input is low. The modified logic is better than domino logic since it does not require an inverter for cascading the gates. In pre-discharging, resetting the output low prevents the problems of charge sharing and charge leakage associated with the other dynamic logic families and also avoids the static power dissipation which exists in the low power dynamic logic. Also resetting the output low avoids the problem of high transition time from high level to low level which exists in circuits employing PMOS logic. The proposed circuit is a mix of PMOS logic and a dynamic logic. The proposed logic cell can be cascaded in a domino like fashion without the need of an inverter.

Reference


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