Abstract

Test power and test time have been the major issues for current scenario of VLSI testing. The test data compression is the well known method used to reduce the test time. The don’t care bit filling method can be used for effective test data compression as well as reduction in scan power. In this paper we describe the algorithm for don’t care assignment like MT (Minimum
Transition)-fill technique and hamming distance based technique. The selective Huffman, optimal Huffman and modified selective Huffman coding are applied on the mapping set to give the optimum Compression and weighted transition matrix is used for scan power. Using these techniques find compression and scan power parameters like average power and peak power and conclude that MT-fill technique gives low peak and average powers and Hamming distance based modified selective Huffman coding technique gives higher compression ratio compare to another methods like selective and optimal Huffman coding.

Reference

- K.A.Bhavsar Mehta U(2011), Analysis of Test Data Compression Techniques Emphazing Statistical Coding Schemes:proceeding in ACM Digital Library USA

Index Terms

Computer Science

Circuits
### Key words

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<tr>
<th>Data Compression</th>
<th>IP Core based SoC</th>
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Don't Care Bit Filling

- MT-fill technique
- Hamming distance based technique
- Switching activity
- Peak power
- Average power