Abstract

Digital images are often contaminated by noise, which degrades their visual and information quality sternly. Images can be corrupted at any stage of its acquisition and transmission through the medium. Image denoising is an essential process intended to eliminate the noise from naturally corrupted images. Wavelets were proved to be an excellent solution to denoising problems due to its remarkable capability in parallel time-frequency analysis. The wavelet transforms are based on shrinking the wavelet coefficients. Though, the Discrete Wavelet Transform (DWT) is an efficient tool, it suffers with specific limitations which reduced its use in many applications. Kingsbury introduced a redundant complex wavelet transform to avoid the limitations in standard DWT. Addressing this case various algorithms were emerged as a result of the vast research in this domain. However, in that work, the de-noising scheme was only realized in software manner. This work focuses on the hardware realization of a real-time wavelet de-noising procedure. The proposed de-noising method mainly consists of three modules: a DTCWT, a thresholding, and inverse DTCWT modular circuits. Two stage 2D-DTCWT based image denoising has been performed using soft thresholding method and
then the hardware software co-simulation design has been synthesized in Xilinx ISE 14.5 and implemented on vertex 5 FPGA kit which operates at a frequency of 207.771MHz.

References


Index Terms

Computer Science  Image Processing

Keywords

DTCWT, Denoising, Soft-thresholding, PSNR, and FPGA
VLSI Implementation of Image Denoising Algorithm using Dual Tree Complex Wavelet Transform