# Study of Complexity of Structural Relation for Interconnection Network 

Mamta<br>Research Scholar, APS University Rewa, M.P

Manish Bhardwaj<br>Senior Scientist, Csir,<br>HRD Group, New Delhi,

Rakesh Kumar Katare
Dept. of computer Science,
APS University, Rewa, M.P


#### Abstract

In this paper, we analyze the connectivity matrix of vertexvertex, vertex-edge, edge-edge. The bit matrix shows some unique relation between vertex-edge. Observation of these matrix pattern shows equivalence relation, tautology, inverse relation ,diagonal relation in the connectivity matrix.


## Keywords

Connectivity matrix, Tautology, Inverse relation, Equivalence relation

## 1. INTRODUCTION

Complexity of any network depends upon its interconnection architecture and interconnection network architecture can be better represented as connectivity matrix. The connectivity matrix will be very useful to analyze the various architectural properties of network. We can depict some important relationship properties of various interconnected network processors. The network can be represented as graph with node as processor and communication link as edges. And Graph can be stored as adjacency matrix. Bit pattern representation of connectivity matrix shows the way of mapping data between two or more communicating processor node in a network

## 2. INTERCONNECTION NETWORK WITH FOUR PROCESSING NODE AND FOUR COMMUNICATION LINKS CAN BE REPRESENTED AS

Table 1: Vertex-edge

|  | $e_{0}$ | $e_{1}$ | $e_{2}$ | $e_{3}$ |
| :---: | :---: | :---: | :---: | :---: |
| $v_{0}$ | 1 | 0 | 0 | 1 |
| $v_{1}$ | 1 | 1 | 0 | 0 |
| $v_{2}$ | 0 | 1 | 0 | 1 |
| $v_{3}$ | 0 | 0 | 1 | 1 |



Fig 1: Graphical representation with four nodes

Table 2: Vertex-Vertex

|  | $\mathrm{v}_{0}$ | $\mathrm{v}_{1}$ | $\mathrm{v}_{2}$ | $\mathrm{v}_{3}$ |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{v}_{0}$ | 0 | 1 | 0 | 1 |
| $\mathrm{v}_{1}$ | 1 | 0 | 1 | 0 |
| $\mathrm{v}_{2}$ | 0 | 1 | 0 | 1 |
| $\mathrm{v}_{3}$ | 1 | 0 | 1 | 0 |

Table 3: Edge-Edge

|  | $e_{0}$ | $e_{1}$ | $e_{2}$ | $e_{3}$ |
| :---: | :---: | :---: | :---: | :---: |
| $e_{0}$ | 0 | 1 | 0 | 1 |
| $e_{1}$ | 1 | 0 | 1 | 0 |
| $e_{2}$ | 0 | 1 | 0 | 1 |
| $e_{3}$ | 1 | 0 | 1 | 0 |

Table 4: Relationship matrix between Vertex - Edge.

| $\mathrm{e}_{1}$ | $\mathrm{e}_{1}{ }^{\prime}$ | $\mathrm{e}_{3}$ | $\mathrm{~V}_{4}$ | $\mathrm{~V}_{4}{ }^{\prime}$ | $\left[\mathrm{V}_{4}\right]^{\top}$ | $\mathrm{e}_{3}$ | $\mathrm{e}_{3}{ }^{\top}$ | $\mathrm{V}_{2}$ | $\mathrm{e}_{3} \Leftrightarrow \mathrm{e}_{3}^{\top}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |

Table 5: Equivalence Matrix of Vertex - Edge

| $\mathrm{e}_{1}$ | $\mathrm{e}_{1}^{\prime}$ | $\mathrm{e}_{1} \Leftrightarrow \mathrm{e}$ <br> $1^{\prime}$ | $\left[\mathrm{v}_{4}\right]^{\top}$ | $\mathrm{e}_{3}{ }^{\top}$ | $\left[\mathrm{e}_{4}\right]^{\top} \Leftrightarrow$ <br> $\left[\mathrm{e}_{3}\right]^{\top}$ |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 1 |

Theorem1: In equivalence,Contradiction shows compliment of each other contrary exclusion shows tautology.

The relationship derived from the above matrix, it is clear that equivalence relation is contradiction with the same vertex and edge. Theorem says that connectivity of vertex with edges can be improved by implementing the above deduction.

Lemma1: A method of connectivity between processors shows the way of mapping data between processors. The exploitation of connectivity through a mathematical model .

Lemma2: Tautology shows same pairs on equivalence.

## 3. PARTITIONING MATRIX

The vertex-edge partitioning matrix shows diagonal balancing of the interconnection network architecture of four
node and four edge. This relationship is valid for equal number of vertices and edges.

|  | $\mathrm{e}_{1}$ | $\mathrm{e}_{2}$ | $\mathrm{e}_{3}$ | $\mathrm{e}_{4}$ |
| :--- | :--- | :--- | :--- | :--- |
| $\mathrm{~V}_{1}$ | 1 | 0 | 0 | 1 |
| $\mathrm{~V}_{2}$ | 1 | 1 | 0 | 0 |
| $\mathrm{v}_{3}$ | 0 | 1 | 1 | 0 |
| $\mathrm{v}_{4}$ | 0 | 0 | 1 | 1 |

Fig 2: vertex-edge
In vertex-vertex partitioning matrix shows diagonal balancing of load.

|  | $\mathrm{v}_{1}$ | $\mathrm{v}_{2}$ | $\mathrm{v}_{3}$ | $\mathrm{v}_{4}$ |
| :--- | :--- | :--- | :--- | :--- |
| $\mathrm{~V}_{1}$ | 0 | 1 | 0 | 1 |
| $\mathrm{v}_{2}$ | 1 | 0 | 1 | 0 |
| $\mathrm{v}_{3}$ | 0 | 1 | 0 | 1 |
| $\mathrm{v}_{4}$ | 1 | 0 | 1 | 0 |

Fig 3: vertex-vertex Partitioning Matrix
Also the edge-edge partitioning matrix show a balancing pattern of load.

|  | $\mathrm{e}_{1}$ | $\mathrm{e}_{2}$ | $\mathrm{e}_{3}$ | $\mathrm{e}_{4}$ |
| :--- | :--- | :--- | :--- | :--- |
| $\mathrm{e}_{1}$ | 0 | 1 | 0 | 1 |
| $\mathrm{e}_{2}$ | 1 | 0 | 1 | 0 |
| $\mathrm{e}_{3}$ | 0 | 1 | 0 | 1 |
| $\mathrm{e}_{4}$ | 1 | 0 | 1 | 0 |

Fig 4: edge- edge
The above relation is valid for equal number of edges and vertices.

Vertex-edge matrix is diagonally compliment i.e. off diagonal upper lower triangular diagonal matrix are compliment to each other where as vertex-vertex and edge-edge matrix are diagonally same means vertex-vertex \& edge-edge shows tautologically on equivalence (i.e contradiction on mutual exclusion) but vertex-edge are tautological on exclusion (i.e. contradiction on equivalence)

Theorem 2: The robustness property of interconnection network is studies on the basis of its structural properties.

## Vertex-edge matrics

$\left.\begin{array}{llllllll}\mathrm{e}_{1}= \\ \mathrm{e}_{1}{ }^{\prime}= \\ {\left[\mathrm{v}_{4}\right]^{\mathrm{T}}=\mathrm{v}_{4}=} \\ {\left[\mathrm{e}_{3}\right]^{\mathrm{T}}=\mathrm{e}_{3}=\left[\begin{array}{lllllll}1 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0\end{array}\right]} \\ {\left[\begin{array}{lllll}1 & 0 & 0 & 1 & 1\end{array}\right.} & 0 & 1 & 1\end{array}\right]$

| edge - edge |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
| $\mathrm{e}_{1}=$ | [0 | 1 | 0 | 1] |
| $\mathrm{e}_{1}{ }^{\prime}=$ | [1 | 0 | 1 | $0]$ |

Vertex-vertex
$\left[\mathrm{V}_{4}\right]^{\mathrm{T}}=\mathrm{V}_{4}=\left[\begin{array}{llll}1 & 0 & 1 & 0\end{array}\right]$
Edge-Edge
$e_{3}=\quad\left[\begin{array}{llll}0 & 1 & 0 & 1\end{array}\right]$
Edge- vertex matrix is the best matrix for the study of connectivity and complexity.

The following observation is made on the connectivity matrix.
i) The vertex-edge matrix shows column-wise connectivity for vertex and row wise Connectivity for edges.
ii) Vertex-vertex matrix parallel diagonal shows the processor node connectivity.
iii) Edge-edge matrix parallel diagonal shows the communication link with other links in a network.
iv) Diagonal in the vertex-vertex and edge-edge shows the interconnection network is self loop free
v) The number of 1 of each row show the connection with the vertex.
vi) Same bit pattern of column shows parallel edges.
vii) Lemma 3:A bit patter represented by connectivity matrix shows the way of mapping between various processors.
viii) Now, the state transition table represent the transition of processing node.
ix) Connectivity pattern can be represented by the following table


Fig 5: Transition Diagram
From the bit pattern we observed that the connectivity of the processor node $\mathrm{p}_{0}$ and $\mathrm{p}_{2}$ is same where as the connectivity of processor $p_{1}$ and $p_{3}$ is same which shows that if node value is same then they will not be connected to each other.
Efficiency of one node $=$ (total number of communication links /total possible communication link) $* 100=(2 / 16) * 100$
The efficiency of connectivity of ICN with four nodes can be calculated as $(8 / 16)^{*} 100$ is $50 \%$.

## 4. INTERCONNECTION NETWORK PDN STRUCTURE HAVING SEVEN NODES

The graphical representation of PDN with seven nodes can be represented as


5
Fig 6: PDN Structure

Table 7: vertex-vertex connectivity matrix of PDN

|  | $\mathrm{P}_{0}$ | $\mathrm{P}_{1}$ | $\mathrm{P}_{2}$ | $\mathrm{P}_{3}$ | $\mathrm{P}_{4}$ | $\mathrm{P}_{5}$ | $\mathrm{P}_{6}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{P}_{0}$ | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| $\mathrm{P}_{1}$ | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| $\mathrm{P}_{2}$ | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| $\mathrm{P}_{3}$ | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| $\mathrm{P}_{4}$ | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| $\mathrm{P}_{5}$ | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| $\mathrm{P}_{6}$ | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

The efficiency of perfect difference network is proposed on the density of communication link
We consider the PDN for $\mathrm{d}=2$ value. PDN is based on perfect different $\operatorname{set}\left\{\mathrm{s}_{0}, \mathrm{~s}_{1}, \mathrm{~s}_{2} \ldots \ldots \mathrm{~s} \delta\right\}$ having node

Table 8: State Table

| Nodes | With other node <br> $\mathrm{P}_{0} \mathrm{p}_{1} \mathrm{p}_{2} \mathrm{p}_{3} \mathrm{p}_{4} \mathrm{p}_{5} \mathrm{p}_{6}$ |
| :---: | :---: |
| $\mathrm{P}_{0}$ | 0101101 |
| $\mathrm{P}_{1}$ | 1010110 |
| $\mathrm{P}_{2}$ | 0101011 |
| $\mathrm{P}_{3}$ | 1010101 |
| $\mathrm{P}_{4}$ | 1101010 |
| $\mathrm{P}_{5}$ | 0110101 |
| $\mathrm{P}_{6}$ | 1011010 |

Table 9: connectivity matrix of vertex edges

|  | $\mathrm{e}_{0}$ | $\mathrm{e}_{1}$ | $\mathrm{e}_{2}$ | $\mathrm{e}_{3}$ | $\mathrm{e}_{4}$ | $\mathrm{e}_{5}$ | $\mathrm{e}_{6}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{0}$ | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| V 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| V 2 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| V 3 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| V 4 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| V 5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| V 6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Tab 10: Diagonal relationship of vertex-vertex with edge

|  | $\mathrm{V}_{0}$ | $\mathrm{~V}_{1}$ | $\mathrm{~V}_{2}$ | $\mathrm{~V}_{3}$ | $\mathrm{~V}_{4}$ | $\mathrm{~V}_{4}$ | $\mathrm{~V}_{6}$ |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| $\mathrm{~V}_{0}$ | 0 | $\mathrm{e}_{0}$ |  |  |  |  |  |
| $\mathrm{~V}_{1}$ | $\mathrm{e}_{0}$ | 0 | $\mathrm{e}_{1}$ |  |  |  |  |
| $\mathrm{~V}_{2}$ |  | $\mathrm{e}_{1}$ | 0 | $\mathrm{e}_{2}$ |  |  |  |
| $\mathrm{~V}_{3}$ |  |  | $\mathrm{e}_{2}$ | 0 | $\mathrm{e}_{3}$ |  |  |
| $\mathrm{~V}_{4}$ |  |  |  | $\mathrm{e}_{3}$ | 0 | $\mathrm{e}_{4}$ |  |
| $\mathrm{~V}_{5}$ |  |  |  |  | $\mathrm{e}_{4}$ | 0 | $\mathrm{e}_{5}$ |
| $\mathrm{~V}_{6}$ |  |  |  |  |  | $\mathrm{e}_{5}$ | 0 |

From the above matrix we can deduce following relationship between row and connected column which is summarized as:
i) $\quad V_{0}$ and $V_{6}$ are connected diagonally with $e_{7}$ and $e_{13}$
ii) $V_{0}$ and $v_{1}$ are connected diagonally through $e_{8}$, and $e_{9}$
iii) $v_{1}$ and $v_{2}$ are connected diagonally through $e_{1 o}$ and $e_{11}$
iv) $V_{2}$ and $v_{3}$ diagonally connected through $e_{12}$ and $e_{13}$
v) $\mathrm{V}_{5}$ and $\mathrm{v}_{6}$ are connected diagonally through $\mathrm{e}_{11}$ and $\mathrm{e}_{12}$
vi) $V_{3}$ and $v_{4}$ are connected diagonally through $e_{7}$ and $e_{8}$.
vii) $V_{4}$ and $v_{5}$ are connected diagonally through $e_{9}$ and $e_{10}$.

Table 11:Diagonal matrix shows the Fabric property of PDN network architecture

|  | $\mathrm{e}_{7}$ | $\mathrm{e}_{8}$ | $\mathrm{e}_{9}$ | $\mathrm{e}_{10}$ | $\mathrm{e}_{11}$ | $\mathrm{e}_{12}$ | $\mathrm{e}_{13}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{~V}_{0}$ | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| $\mathrm{~V}_{1}$ | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| $\mathrm{~V}_{2}$ | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| $\mathrm{~V}_{3}$ | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| $\mathrm{~V}_{4}$ | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| $\mathrm{~V}_{5}$ | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| $\mathrm{~V}_{6}$ | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

$\boldsymbol{\alpha} \beta$ property of matrix
$\beta=\mathrm{v}_{0}, \mathrm{v}_{1}, \mathrm{v}_{2}, \mathrm{v}_{3}$,
$\mathrm{e}_{7}=\{1,0,0,0,0,0,1\} \quad$ Main diagonal of vertex edge matrix
$\mathrm{e}_{7}=\left\{1,1,0,0,0,{ }^{\circ}\right\} \quad$ Shows vertex $\left(\mathrm{V}_{0}\right)$ and edge $\left(\mathrm{e}_{7}\right)$ inverse relationship
$\mathrm{v}_{0}=\{0,0,0,0,1,1\}$
$\mathrm{e}_{8}=\{0,1,1,0,0\}$
$\mathrm{V}_{1}=\{0,0,1,1,0\}$
$\left.\mathrm{e}_{9}=\underset{\substack{ \\\{0,0,1,1\}}}{\mathrm{V}_{2}=\underset{, 1,0,0\}}{ }}\right]$
Shows vertex $\left(\mathrm{V}_{1}\right)$ and edge $\left(\mathrm{e}_{8}\right)$ inverse relationship
Shows vertex $\left(\mathrm{V}_{2}\right)$ and edge $\left(\mathrm{e}_{9}\right)$ inverse relationship $\left.\left.V_{6}=\boldsymbol{O}, 0,0, \varnothing, \mp\right)\right\}$
$\mathrm{V}_{1}=\{0,0,1,1,0,0,0\}$
$W_{5}=\{0,0,0,1,1,0,0\}$
$V_{2}=\{0,0,0,0,1,1,0\}$


$V_{0}$ and $V_{3}$ are dividing matrix vector.

Fabric properties of PDN both divides the interconnection network in two equal parts

$\left(\left(\mathrm{V}_{0}\{1100000\} \& \mathrm{~V}_{1}\{0011000\}\right) \&\left(\mathrm{e}_{8}\{1000100\} \& \mathrm{e}_{9}\{0100100\}\right)\right.$


The above studies of connectivity matrix of vertex-vertex, vertex-edge and edge-edge shows some unique relationship in an interconnection network. Transition of state is possible at bit position one. An inverse relationship were deduced between vertex-edge and vertex- vertex. The vertex-edge partitioning matrix shows diagonal balancing of the interconnection network architecture in four node and four edge. We have also presented the load balancing for PDN structure.

## 5. CONCLUSION

We can analyze various types of relationship between vertex-vertex, vertex-edges and edge-edge in connectivity matrix. Connectivity matrix shows some important properties of interconnection network. We deduce diagonal and inverse relationship between vertex-edge connectivity matrix.

## 6. REFERENCES

[1] Singer, J. "A theorem in Finite Projective Geometry and Some Applications to Number Theory". Trans American Mathematical Society, Vol.43,pp377385,1938.
[2] Parhami, Behrooz and Rakaov, Mikhail."Perfect Difference Networks and Related Interconnection structures for Parallel and Distributed Systems". IEEE Journal on Parallel and Distributed Systems 16(8):725736, 2005.
[3] Katare, R.K. and Chaudhari, N.S "Study of Topological Property of Interconnection Networks and its mapping to Sparse Matrix Model", International Journal of Computer Science and Applications,2009Technomathematics ResearchFoundation.Vol. 6, No. 1, pp. 26-39.
[4] Katare, R.K and Chaudhari, N.S. "A Comparative study of hypercube and perfect difference network for parallel and distributed systems and its application to sparse linear system". Vladimir Journal of Computer Information Sciences, Vol2, Sandipani Academy, Ujjain(M.P.),India pp13-30,2007.
[5] Wankar, Priyanka, Sharma, Anand, Sinhal, Ruchika "Performance Analysis and Implementation Perfect Difference Network
[6] Tiwari, S., Katare, R.K." A Study of Hex-cell, complete graph and Perfect Difference Network (PDN), 2ndInternational Conference on Emerging Trends in computer science, communication and information Technology,ISBN978-81-923487-1-1(2015).
[7] Tiwari Sunil, Katare R.K.,"A Study of Fabric of Architecture Using Structural Pattern and Relation",

International journal of latest technology in engineering, management and applied science, ISSN No.2278$2540, \mathrm{p}-33-37$, vol IV Issue IX Sep. 2015.
[8] Rakov, M. And J. Machall, "Method of Interconnection Functional Nodes and a Hyperstar I [Rako98] Rakov, M., "Method Of Interconnecting Nodes and a Hyperstar Interconnection Structure ," US Patent 5734 580, issued March 1998.
[9] Parhami B. and Rakov M.A., "Perfect Difference Networks and Related Interconnection Structures for Parallel and Distributed Systems," IEEE Transactions on Parallel and Distributed Systems, Vol. 16, No. 8 , August 2005.
[10] Tiwari S., Katare R.K., "Alliance Study of Perfect Difference Network \& Hex-Cell Architecture". International Journal of Emerging Technology and Advanced Engineering, volume 5,Issue 3, march 2015 p25.
[11] Katare Rakesh, Tiwari Sunil, "Hamiltonian, Topological properties of Hex-Cell and Perfect Difference Network (PDN) for design new Hybrid Architecture for Parallel System," National Seminar on Recent Trends in Science and Technology", March 3031, 2015 , MPCST, Bhopal(M.P.)
[12] P. Guerrier and A. Grenier, "A Generic Architecture for on Chip Packet switched Interconnections," In Proc. Design Automation and Test in Europe Conf. (DATE), pp. 250-256,2000.
[13] Patrikar Rajendra and Gaikwad M., "Perfect Difference Network for Network Chip Architecture," International Journal of C.S., Vol.9, Dec. 2009

